DESCRIPTION

PT6314 is a VFD Controller/Driver IC utilizing CMOS technology providing 80 segment outputs and 24 grid outputs. It supports dot matrix displays of up to 16 columns x 2 lines, 20 columns x 2 lines or 24 columns x 2 lines. PT6314 also features a character generator ROM which stores 248 x 5 x 8 dos characters. Pin assignments and application circuits are optimized for easy PCB layout and cost saving advantages.

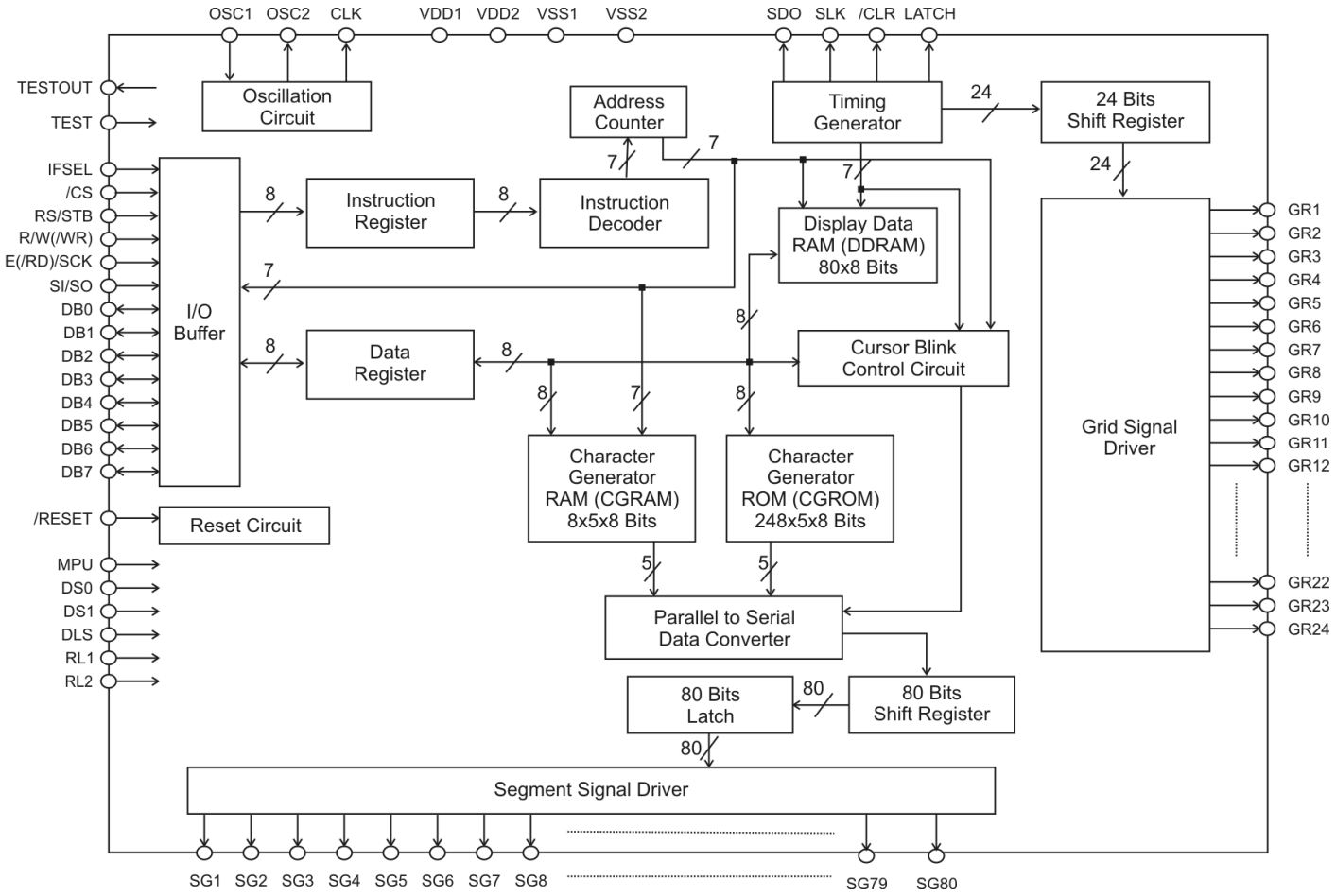
APPLICATIONS

- Electronic equipment with VFD display
- Microprocessor peripherals

FEATURES

- CMOS technology
- Provides up to 80 x 8 display RAM
- Capable of driving segment for cursor displays (48 units)
- Built-in oscillation circuit
- Parallel data input/output (switchable 4 or 8 bits) or serial data input/output
- Alphanumeric and symbolic display via the built-in ROM (5 x 8 dots): 248 characters
- Eight user-defined 5 x 8 dot character CGRAM
- Display contents capability:
  - 16 columns x 2(1) rows + 32(16) cursors
  - 20 columns x 2(1) rows + 40(20) cursors
  - 24 columns x 2(1) rows + 48(24) cursors
- Custom ROM available (please contact PTC

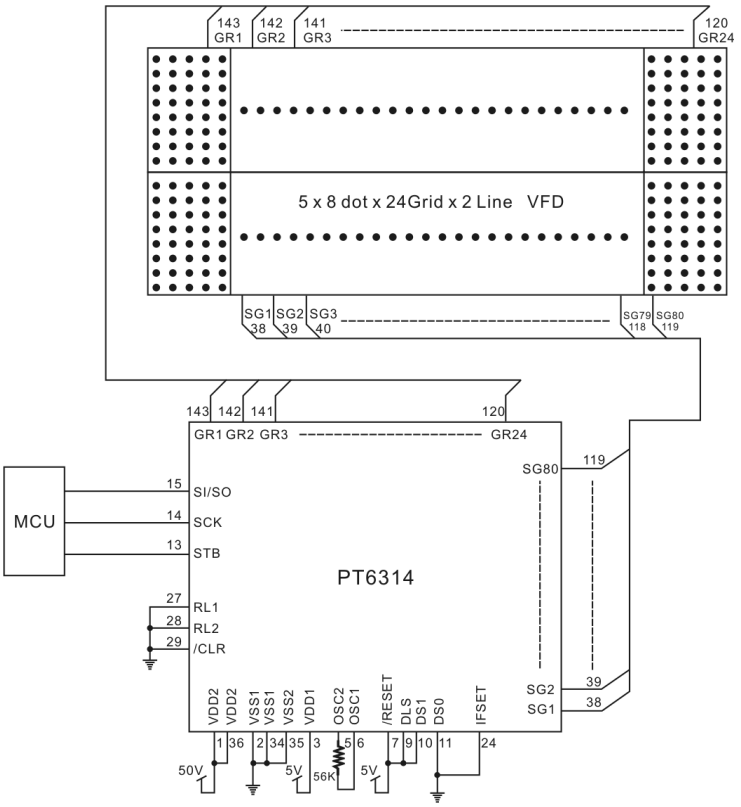
BLOCK DIAGRAM



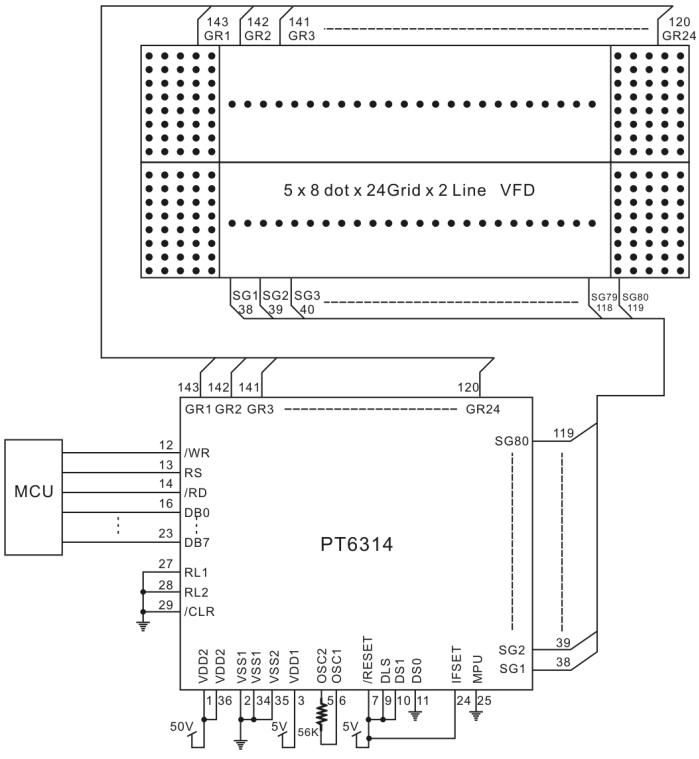
CONTENTS

1. APPLICATION CIRCUITS

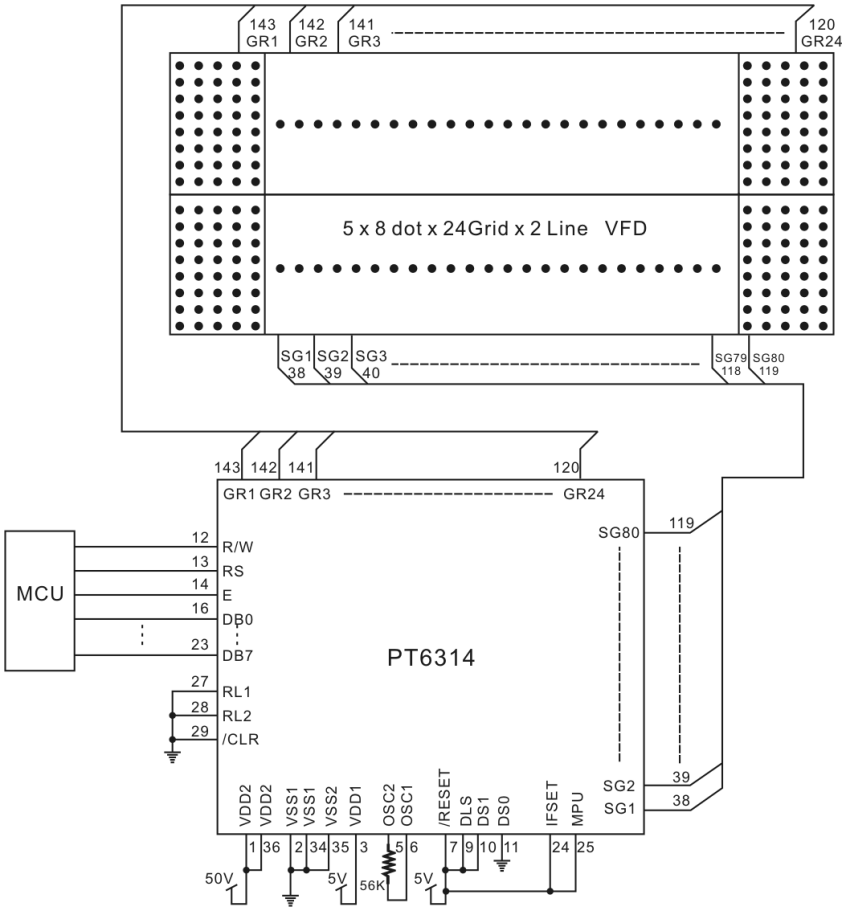
1.1 SERIAL INTERFACE



1.2 i80 INTERFACE



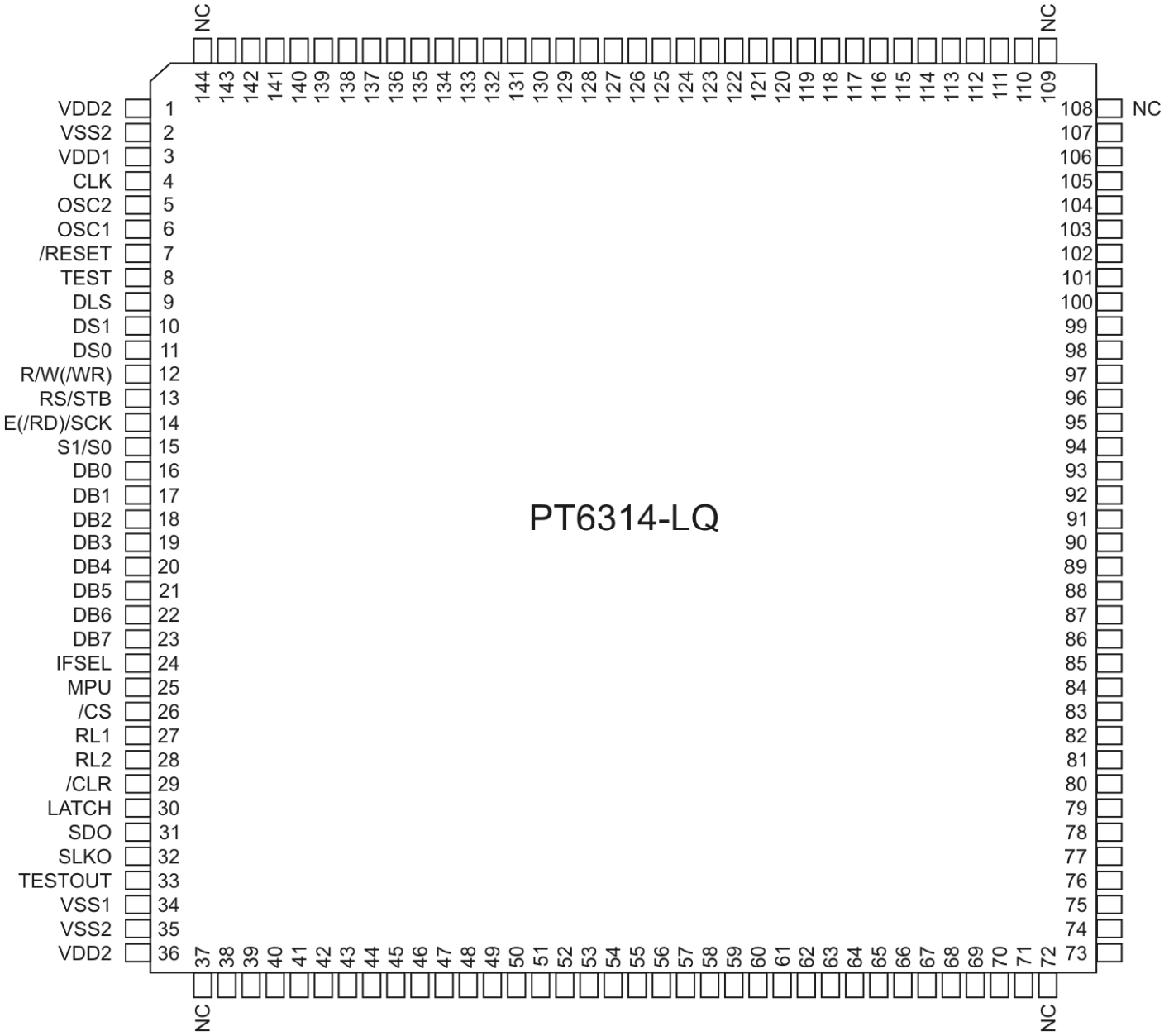
1.3 M68 INTERFACE



2. ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6314-001	144 Pins, LQFP	PT6314-001
PT6314-002	144 Pins, LQFP	PT6314-002
PT6314-007	144 Pins, LQFP	PT6314-007
PT6314-008	144 Pins, LQFP	PT6314-008

3. PIN CONFIGURATION



Note: Pin No. 38 to 71, 73 to 107, 110 to 119 are used as Segment Signal Output Pins, Pin No.120 to 143 are used as Grid Signal Output Pins and are configured according to the Tables shown in the Duty Ratio Setting Section (see pages 8 to 13).

4. PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
VDD2	-	VFD Driving Power Supply Pin	1, 36
VSS2	-	VFD Driving Power Supply Pin	2, 35
VDD1	-	Logic Power Supply Pin	3
CLK	O	Oscillation Signal Output Pin	4
OSC2	O	Oscillation Output Pin	5
OSC1	I	Oscillation Input Pin	6
/RESET	I	Reset Pin When this pin is set to “0”, all internal registers and commands are initialized. The Segment and Grid Outputs are fixed to VDD.	7
TEST	I	Test Pin 0 or floating : the Normal Operation Mode 1:the Test Mode is active	8
DLS	I	Display Line Select Pin This pin is used to select the number of display lines when the Power is ON, Reset or Resetting. 0: 1 line is selected (N=”0”)* 1: 2 lines are selected (N=”1”)*	9
DS1, DS0	I	Duty Select Pin These pins set the duty ratio. The duty ratio is determined by the number of Grid.	10, 11
R/W(/WR)	I	Read/Write (Write) Signal Pin Under the M68 Parallel Data Transfer Mode (R/W), this pin functions as the Data Transfer Select Pin. 0: Write Function 1: Read Function Under the i80 parallel data Transfer Mode (/WR), thispin is Write Enable Pin. It writes data at the rising edge of this signal. Under the Serial Transfer Mode, the Read or Write function is selected by instruction and this pin is connect to either “H” or “L”.	12
RS/STB	I	Register Select/Strobe Pin Under the Parallel Transfer Mode is selected, this pin acts as the Register Select Pin. 0: Instruction Register (IR) 1: Data register (DR) Under Serial Data Transfer Mode, this pin acts as the Strobe Input Pin.	13
E(/RD)/SCK	I	Enable (Read)/Shift Clock Under the M68 Parallel Data Transfer Mode (E), this pin functions as the Write Enable Pin. Data is written at the falling edge. Under the i80 Parallel Data Transfer Mode (/RD), this pin functions as the Read Enable Pin. When this pin is set to “LOW”, data is outputted to the Data Bus. Under the Serial Data Transfer Mode, this pin functions as the Shift Clock Input Pin. Data is written at the rising edge.	14
SI/SO	I/O	Serial Input/Output Pin Under the Serial Data Transfer Mode, this pin functions as an I/O Pin. Under the Parallel Data Transfer Mode, this pin may be connected to either “H” or “L”	15
DB0 to DB7	I/O	Parallel Data Input/Output Pins Under the Parallel Data Transfer Mode, these pins are used as I/O Pin. Under the 4-bit Transfer Mode, DB4 to DB7 are used.	16-23
IFSEL	I	I/F Select Pin This pin is used to select the I/F mode: Serial or Parallel Transfer 0: Serial Data Transfer 1: Parallel Data Transfer	24
MCU	I	Interface Select Pin This pin is used to select the interface mode: i80 or M68. 0: i80 CPU Mode 1: M68 CPU Mode	25
/CS	I	Chip Select Pin When this pin is set to “L” the PT6314 is active.	26

Pin Name	I/O	Description	Pin No.
RL1,RL2	I	Segment Output Select Pin This pins are used to set SG1 to SG80.	27, 28
/CLR	O	Extension Grid Driver Clear Signal Output Pin Active: Low The Grid Data stored in extension driver latch are outputted when this pin is set to “HIGH”. If this pin is set to ”LOW”, the extension driver outputs LOW.	29
LATCH	O	Extension Grid Driver Latch Enable Signal Output Pin	30
SDO	O	Extension Grid Driver Serial Data Output Pin	31
SLK O		Extension Grid Driver Shift Clock Output Pin Rising Edge: Active	32
TESTOUT	O	Test Pin for IC Testing only. This pin should be “open”.	33
VSS1	-	Logic Ground Pin	34
GR1 to GR24	O	Grid Signal Output Pins	143-120
SG1 to SG80	O	Segment Signal Output Pins	see (2)

Notes:
1. *=N is the Display Line Select Flag in “Function Set” Command
2. Refer to Duty Ratio Setting Section

4.1 DUTY RATIO SETTING

DS0 and DS1 control the duty ratio of PT6314. Please refer to the table below.

DS0	DS1	DUTY RATIO
0	0	1/16 (No. of GRID=16)
0	1	1/24 (No. of GRID=24)
1	0	1/20 (No. of GRID=20)
1	1	1/40 (No. of GRID=40)

Please take note that the external extension grid driver is needed to set up 1/40 duty mode.

4.2 SEGMENT SETTING

CONDITION 1: 2-LINE DISPLAY (N="1"), RL1="0" AND RL2="0Z"

The number of Segment Pins is controlled by the RL1 and RL2.

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
SG1	38	SG18	55	NC	72	SG51	89
SG2	39	SG19	56	SG35	73	SG52	90
SG3	40	SG20	57	SG36	74	SG53	91
SG4	41	SG21	58	SG37	75	SG54	92
SG5	42	SG22	59	SG38	76	SG55	93
SG6	43	SG23	60	SG39	77	SG56	94
SG7	44	SG24	61	SG40	78	SG57	95
SG8	45	SG25	62	SG41	79	SG58	96
SG9	46	SG26	63	SG42	80	SG59	97
SG10	47	SG27	64	SG43	81	SG60	98
SG11	48	SG28	65	SG44	82	SG61	99
SG12	49	SG29	66	SG45	83	SG62	100
SG13	50	SG30	67	SG46	84	SG63	101
SG14	51	SG31	68	SG47	85	SG64	102
SG15	52	SG32	69	SG48	86	SG65	103
SG16	53	SG33	70	SG49	87	SG66	104
SG17	54	SG34	71	SG50	88	SG67	105
SG68	106	SG77	116	GR18	126	GR8	136
SG69	107	SG78	117	GR17	127	GR7	137
SG70	108	SG79	118	GR16	128	GR6	138
NC	109	SG80	119	GR15	129	GR5	139
SG71	110	GR24	120	GR14	130	GR4	140
SG72	111	GR23	121	GR13	131	GR3	141
SG73	112	GR22	122	GR12	132	GR2	142
SG74	113	GR21	123	GR11	133	GR1	143
SG75	114	GR20	124	GR10	134	NC	144
SG76	115	GR19	125	GR9	135		

CONDITION 2: 2-LINE DISPLAY (N="1"), RL1="0", RL2="1"

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
SG40	38	SG23	55	NC	72	SG51	89
SG39	39	SG22	56	SG6	73	SG52	90
SG38	40	SG21	57	SG5	74	SG53	91
SG37	41	SG20	58	SG4	75	SG54	92
SG36	42	SG19	59	SG3	76	SG55	93
SG35	43	SG18	60	SG2	77	SG56	94
SG34	44	SG17	61	SG1	78	SG57	95
SG33	45	SG16	62	SG41	79	SG58	96
SG32	46	SG15	63	SG42	80	SG59	97
SG31	47	SG14	64	SG43	81	SG60	98
SG30	48	SG13	65	SG44	82	SG61	99
SG29	49	SG12	66	SG45	83	SG62	100
SG28	50	S G11	67	SG46	84	SG63	101
SG27	51	SG10	68	SG47	85	SG64	102
SG26	52	SG9	69	SG48	86	SG65	103
SG25	53	SG8	70	SG49	87	SG66	104
SG24	54	SG7	71	SG50	88	SG67	105
SG68	106	SG77	116	GR18	126	GR8	136
SG69	107	SG78	117	GR17	127	GR7	137
SG70	108	SG79	118	GR16	128	GR6	138
NC	109	SG80	119	GR15	129	GR5	139
SG71	110	GR24	120	GR14	130	GR4	140
SG72	111	GR23	121	GR13	131	GR3	141
SG73	112	GR22	122	GR12	132	GR2	142
SG74	113	GR21	123	GR11	133	GR1	143
SG75	114	GR20	124	GR10	134	NC	144
SG76	115	GR19	125	GR9	135		

CONDITION 3: 2-LINE DISPLAY (N="1"), RL1="1", AND RL2="0"

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
SG41	38	SG58	55	NC	72	SG30	89
SG42	39	SG59	56	SG75	73	SG29	90
SG43	40	SG60	57	SG76	74	SG28	91
SG44	41	SG61	58	SG77	75	SG27	92
SG45	42	SG62	59	SG78	76	SG26	93
SG46	43	SG63	60	SG79	77	SG25	94
SG47	44	SG64	61	SG80	78	SG24	95
SG48	45	SG65	62	SG40	79	SG23	96
SG49	46	SG66	63	SG39	80	SG22	97
SG50	47	SG67	64	SG38	81	SG21	98
SG51	48	SG68	65	SG37	82	SG20	99
SG52	49	SG69	66	SG36	83	SG19	100
SG53	50	SG70	67	SG35	84	SG18	101
SG54	51	SG71	68	SG34	85	SG17	102
SG55	52	SG72	69	SG33	86	SG16	103
SG56	53	SG73	70	SG32	87	SG15	104
SG57	54	SG74	71	SG31	88	SG14	105
SG13	106	SG4	116	GR18	126	GR8	136
SG12	107	SG3	117	GR17	127	GR7	137
SG11	108	SG2	118	GR16	128	GR6	138
NC	109	SG1	119	GR15	129	GR5	139
SG10	110	GR24	120	GR14	130	GR4	140
SG9	111	GR23	121	GR13	131	GR3	141
SG9	112	GR22	122	GR12	132	GR2	142
SG7	113	GR21	123	GR11	133	GR1	143
SG6	114	GR20	124	GR10	134	NC	144
SG5	115	GR19	125	GR9	135		

CONDITION 4: 2-LINE DISPLAY (N="1"), RL1="1" AND RL2="1"

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
SG80	38	SG63	55	NC	72	SG30	89
SG79	39	SG62	56	SG75	73	SG29	90
SG78	40	SG61	57	SG76	74	SG28	91
SG77	41	SG60	58	SG77	75	SG27	92
SG76	42	SG59	59	SG78	76	SG26	93
SG75	43	SG58	60	SG79	77	SG25	94
SG74	44	SG57	61	SG80	78	SG24	95
SG73	45	SG56	62	SG40	79	SG23	96
SG72	46	SG55	63	SG39	80	SG22	97
SG71	47	SG54	64	SG38	81	SG21	98
SG70	48	SG53	65	SG37	82	SG20	99
SG69	49	SG52	66	SG36	83	SG19	100
SG68	50	SG51	67	SG35	84	SG18	101
SG67	51	SG50	68	SG34	85	SG17	102
SG66	52	SG49	69	SG33	86	SG16	103
SG65	53	SG48	70	SG32	87	SG15	104
SG64	54	SG47	71	SG31	88	SG14	105
SG13	106	SG4	116	GR18	126	GR8	136
SG12	107	SG3	117	GR17	127	GR7	137
SG11	108	SG2	118	GR16	128	GR6	138
NC	109	SG1	119	GR15	129	GR5	139
SG10	110	GR24	120	GR14	130	GR4	140
SG9	111	GR23	121	GR13	131	GR3	141
SG9	112	GR22	122	GR12	132	GR2	142
SG7	113	GR21	123	GR11	133	GR1	143
SG6	114	GR20	124	GR10	134	NC	144
SG5	115	GR19	125	GR9	135		

CONDITION 5:1-LINE DISPLAY (N="0"), RL2="0"

The RL1 setting is irrelevant. The table below shows the Segment Pin setting.

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
SG1	38	SG18	55	NC	72	*	89
SG2	39	SG19	56	SG35	73	*	90
SG3	40	SG20	57	SG36	74	*	91
SG4	41	SG21	58	SG37	75	*	92
SG5	42	SG22	59	SG38	76	*	93
SG6	43	SG23	60	SG39	77	*	94
SG7	44	SG24	61	SG40	78	*	95
SG8	45	SG25	62	*	79	*	96
SG9	46	SG26	63	*	80	*	97
SG10	47	SG27	64	*	81	*	98
SG11	48	SG28	65	*	82	*	99
SG12	49	SG29	66	*	83	*	100
SG13	50	S G30	67	*	84	*	101
SG14	51	SG31	68	*	85	*	102
SG15	52	SG32	69	*	86	*	103
SG16	53	SG33	70	*	87	*	104
SG17	54	SG34	71	*	88	*	105
*	106	*	116	GR18	126	GR8	136
*	107	*	117	GR17	127	GR7	137
*	108	*	118	GR16	128	GR6	138
NC	109	*	119	GR15	129	GR5	139
*	110	GR24	120	GR14	130	GR4	140
*	111	GR23	121	GR13	131	GR3	141
*	112	GR22	122	GR12	132	GR2	142
*	113	GR21	123	GR11	133	GR1	143
*	114	GR20	124	GR10	134	NC	144
*	115	GR19	125	GR9	135		

Note: *=Not Used

CONDITION 6: 1-LINE DISPLAY, RL2="1"

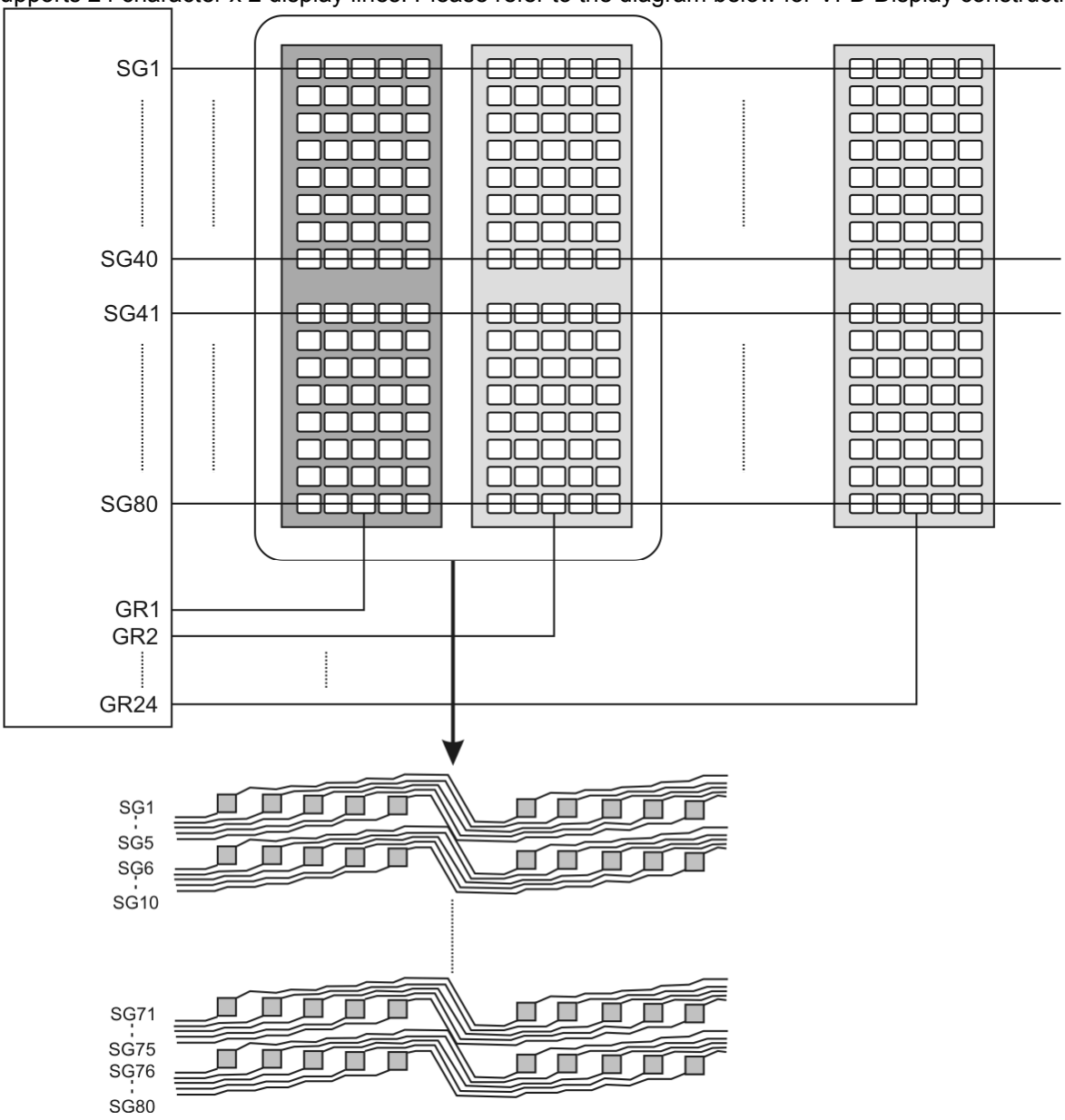
The RL1 setting is irrelevant. Segment Output Pin settings are as follows:

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
SG40	38	SG23	55	NC	72	*	89
SG39	39	SG22	56	SG6	73	*	90
SG38	40	SG21	57	SG5	74	*	91
SG37	41	SG20	58	SG4	75	*	92
SG36	42	SG19	59	SG3	76	*	93
SG35	43	SG18	60	SG2	77	*	94
SG34	44	SG17	61	SG1	78	*	95
SG33	45	SG16	62	*	79	*	96
SG32	46	SG15	63	*	80	*	97
SG31	47	SG14	64	*	81	*	98
SG30	48	SG13	65	*	82	*	99
SG29	49	SG12	66	*	83	*	100
SG28	50	S G11	67	*	84	*	101
SG27	51	SG10	68	*	85	*	102
SG26	52	SG9	69	*	86	*	103
SG25	53	SG8	70	*	87	*	104
SG24	54	SG7	71	*	88	*	105
*	106	*	116	GR18	126	GR8	136
*	107	*	117	GR17	127	GR7	137
*	108	*	118	GR16	128	GR6	138
NC	109	*	119	GR15	129	GR5	139
*	110	GR24	120	GR14	130	GR4	140
*	111	GR23	121	GR13	131	GR3	141
*	112	GR22	122	GR12	132	GR2	142
*	113	GR21	123	GR11	133	GR1	143
*	114	GR20	124	GR10	134	NC	144
*	115	GR19	125	GR9	135		

Note: *=Not Used

4.3 VFD DISPLAY

PT6314 supports 24 character x 2 display lines. Please refer to the diagram below for VFD Display construction.



5. FUNCTION DESCRIPTION

5.1 BLOCK FUNCTIONS

5.1.1 CPU INTERFACE

PT6314 provides either 4 or 8 bits parallel or serial interface. These interface modes may be selected using the IFSEL Pin (Pin No.24) as follows:

IFSEL Setting	Data Transfer Mode
"0"	Serial Data Transfer
"1"	Parallel Data Transfer

5.1.2 REGISTERS (INSTRUCTION REGISTER & DATA REGISTER)

PT6314 supports two 8-bit registers, namely: an Instruction Register (IR) and a Data Register (DR) which may be selected using the Register Selector (RS) Signal. Please refer to Table below

IFSEL	/CS	RS	E/SCK	R/W	MCU	SI/SO	DBn
0	/CS	STB	SCK	*	*	SI/SO	*
1	/CS	RS	E/(/RD)	R/D(/WR)	MCU	*	DBn

Note: *=This pin must be kept in either "HIGH" or "LOW" State.

The Instruction Register (IR) stores (1) instruction codes (i.e. display clear and cursor shift), (2) Display Data RAM (DDRAM) Address Information and (3) Character Generator RAM (CGRAM). It can only be written from the MCU.

The Data Register (DR) acts as a temporary storage for (1) data to be written into the DDRAM or CGRAM and (2) data to be read from the DDRAM or CGRAM. Data written into the DR from the MCU is automatically written into the DDRAM or CGRAM by internal operation. When the data stored in DR is read by the MCU, data transfer is completed. After the completion of the data transfer (that is, after the MCU has finished reading the first set of data), the DDRAM or CGRAM data in the next address is sent to the DR. The MCU then again performs its Read operation for the next set of data.

BUSY FLAG (READ BF FLAG)

The Busy Flag Data (DB7) always outputs "0".

ADDRESS COUNTER (AC)

The Address Counter (AC) designates the addresses of the DDRAM and CGRAM. When an address of instruction is written into the Instruction Register, the address information is sent from the Instruction Register (IR) to the Address Counter. The selection of either the DRAM or CGRAM is also determined concurrently by the instruction. After writing into the DDRAM or CGRAM, the Address Counter is increased by 1. (The Address Counter is decreased by 1 after data is read from the DDRAM or CGRAM.) The contents of the Address Counter are then outputted to the DB0~DB6 when RS="0" and R/W="1". Please refer to the table below.

Common	M68	i80		Register Selection
RS	R/W	/RD	/WR	
0	0	1	0	Write IR Data as internal operation (i.e. display clear)
0	1	0	1	Read data to busy flag (DB7) and Address Counter (DB6 to DB0)
1	0	1	0	Write DR Data (DR→DDRAM/CGRAM)
1	1	0	1	Read DR Data (DDRAM/CGRAM→DR)

5.2 DISPLAY DATA RAM (DDRAM)

The Display Data RAM (DDRAM) stores the display data shown in the 8-bit character codes. When expanded the Display Data RAM supports a capacity of 80 x 8 bits or 80 characters. The area in the DDRAM that is not in used for display may be used as general data RAM.

	High Order Bits			Low Order Bits			
AC	AC6	AC5	AC4	AC3	AC2	AC1	AC0
	hexadecimal			hexadecimal			

Please note that the DDRAM Address (ADD) is set in the Address Counter(AC) as hexadecimal.

Example: DDRAM Address “26”:

0	1	0	0	1	1	0
2			6			

5.2.1 N=“0” 1-LINE DISPLAY, 80 CHARACTERS

Display Position

Digit	1	2	3	4	5	6	……	79	80
DDRAM Address(hexadecimal)	00	01	02	03	04	05	……	4E	4F

5.2.2 N=“0” 1-LINE DISPLAY, LESS THAN 80 CHARACTERS

In cases when there are less than 80 display characters, the display begins at the head position. For example, if only one piece of PT6314 is being used, 24 characters are displayed. When the display shift operation is performed, the DDRAM address shifts, please refer to the figure below.

Display Position

Digit	1	2	3	4	5	6	……	23	24
DDRAM Address(hexadecimal)	00	01	02	03	04	05	……	16	17
For Shift-Left	01	02	03	04	05	06	……	17	18
For Shift-Right	4F	00	01	02	03	04	……	15	16

5.2.3 N=“1” 2-LINE DISPLAY, 40 CHARACTERS

Display Position

Digit	1	2	3	4	5	6	……	39	40
DDRAM Address	00	01	02	03	04	05	……	26	27
(hexadecimal)	40	41	42	43	44	45	……	66	67

5.2.4 N=“1” 2-LINE DISPLAY, LESS THAN 40 CHARACTERS

In cases when the number of display characters is less than 40 x 2 lines, the two lines are displayed from the head. The line end address and the second line start address are not consecutive. For example, if only one PT6314 is being used, 24 characters x 2 lines are displayed. When the display shift operation is performed, the DDRAM address shifts.

Display Position

Digit	1	2	3	4	5	6	……	23	24
DDRAM Address	00	01	02	03	04	05	……	16	17
(hexadecimal)	40	41	42	43	44	45	……	56	57
For Shift-Left	01	02	03	04	05	06	……	17	18
	41	42	43	44	45	46	……	57	58
For Shift-Right	27	00	01	02	03	04	……	15	16
	67	40	41	42	43	44	……	55	56

5.2.5 N="1" 2-LINE DISPLAY, 40 CHARACTERS

PT6314 can be extended using one of the 16 output extension drivers as GRID. Under this condition, a 40-character x 2 lines display may be constructed.

Display Position

Digit	1	2	3	4	……	23	24	25	……	39	40
DDRAM Address (hexadecimal)	00	01	02	03	……	16	17	18	……	26	27
	40	41	42	43	……	56	57	58	……	66	67

Digit	1	2	3	4	……	23	24	25	……	39	40
For Shift-Left	01	02	03	04	……	17	18	19	……	27	00
	41	42	43	44	……	57	58	59	……	67	40

Digit	1	2	3	4	……	23	24	25	……	39	40
For Shift-Right	27	00	01	02	……	15	16	17	……	25	26
	67	40	41	42	……	55	56	57	……	65	66
	PT6314 Display							Extension Driver Display			

5.3 CHARACTER GENERATOR ROM (CGROM)

The CGROM is the Read Only Memory (ROM) responsible for the generation of 5 x 8 dots character patterns from 8-bit character codes. A total of up to 240 character patterns can be generated. Please note that Character Codes -- 00H to 07H are allocated to the CGRAM.

5.4 CHARACTER GENERATOR RAM (CGRAM)

The Character Generator RAM (CGRAM) allows the user to reconstruct the character patterns from 8-bit by software programming. Eight character patterns can be written and constructed using 5 x 8 dots. Areas that are not used for display purposes may be used as general data RAM.

The table below shows the relationship between the CGRAM Address, Character Code (DDRAM) and the 5x7 (cursor included) dot character patterns (CGRAM).

Character Code (DDRAM Data)								CGRAM Address						CGRAM Data								
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
High Order Bit							Low Order Bit	High Order Bit			Low Order Bit			High Order Bit							Low Order Bit	
0	0	0	0	X	0	0	0	0	0	0	0	0	0	X	X	X	1	1	1	1	1	
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				1	1	1	1	1	Character Pattern No. 1
											1	0	0				1	0	0	0	0	
											1	0	1				1	0	0	0	0	
											1	1	0				1	0	0	0	0	
											1	1	1				0	0	0	0	0	Cursor Position
0	0	0	0	X	0	0	1	0	0	1	0	0	0	X	X	X	1	1	1	1	1	
											0	0	1				0	0	1	0	0	
											0	1	0				0	0	1	0	0	
											0	1	1				0	0	1	0	0	Character Pattern No. 2
											1	0	0				0	0	1	0	0	
											1	0	1				0	0	1	0	0	
											1	1	0				0	0	1	0	0	
											1	1	1				0	0	0	0	0	Cursor Position
0	0	0	0	X	1	1	1	1	1	1	0	0	0	X	X	X	0	1	1	1	1	
											0	0	1				1	0	0	0	0	
											0	1	0				1	0	0	0	0	
											0	1	1				1	0	0	0	0	Character Pattern No. 8
											1	0	0				1	0	0	0	0	
											1	0	1				1	0	0	0	0	
											1	1	0				0	1	1	1	1	
											1	1	1				1	1	1	1	1	Cursor Position

Notes:
1. X= Irrelevant
2. Character Code Bits 0 to 2 correspond to the CGRAM Address Bits 3 to 5 (3 bits: 8 type).
3. CGRAM Address Bits 0 to 2 determine the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position at 0 as the cursor display. If the 8th line data is “1” all the 1 bits will light up the 8th line regardless of the cursor presence.
4. Character pattern row position corresponds to the CGRAM data bits 0 to 4. (bit 4 is positioned at the left)
5. The CGRAM character patterns are selected when the character code bits 4 to 7 are all set to “0”. The Character Code Bit 3 is irrelevant, the “P” Display shown above (Character Pattern No. 1) can be selected by either character Code 00H or 07H.
6. When CGRAM Data=“1” the Display is turned ON. When CGRAM data=“0” display is turned OFF.

5.5 TIMING GENERATION CIRCUIT

Timing signals for internal circuit operations(i.e. DDRAM, CGRAM) are generated by the Timing Generation Circuit. The Display RAM Read timing and the MCU access internal operation timing are generated separately in order to avoid interferences. Thus, for example, when data is being written to the DDRAM, no undesirable interference occur (i.e. flickering in areas other than the display location)

5.6 VFD DRIVER CIRCUIT

The VFD Driver Circuit is composed of 24 grid and 80 segment signal drivers. During power On, the character font and number of digits are selected by the hardware (DS0 and DS1), the required grid signal drivers automatically output drive waveforms while the other grid signal drivers continue to output non-selected waveforms. The serial data sent is latched when the display data character pattern corresponding to the last address of the display data RAM (DDRAM). Since the serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, PT6314 drives from the head display.

5.7 CURSOR/BLINK CONTROL CIRCUIT

Cursor and Character blinking are generated by the Cursor / Blink Control Circuit. The cursor or the blinking will appear with the digit located at the display data RAM (DDRAM) address set in the address counter (AC).
For example, when the address counter is 08H, the cursor position is displayed at DDRAM Address 08H.

	AC6	AC5	AC4	AC3	AC2	AC1	AC0
AC	0	0	0	1	0	0	0

5.7.1 FOR 1-LINE DISPLAY:

Display position

Digit	1	2	3	4	5	6	7	8	9	10	11	12
DDRAM Address(hexadecimal)	00	01	02	03	04	05	06	07	08	09	0A	0B

Cursor Position

5.7.2 FOR 2-LINE DISPLAY:

Display position

Digit	1	2	3	4	5	6	7	8	9	10	11	12
DDRAM Address(hexadecimal)	00	01	02	03	04	05	06	07	08	09	0A	0B
	40	41	42	43	44	45	46	47	48	49	4A	4B

Cursor Position

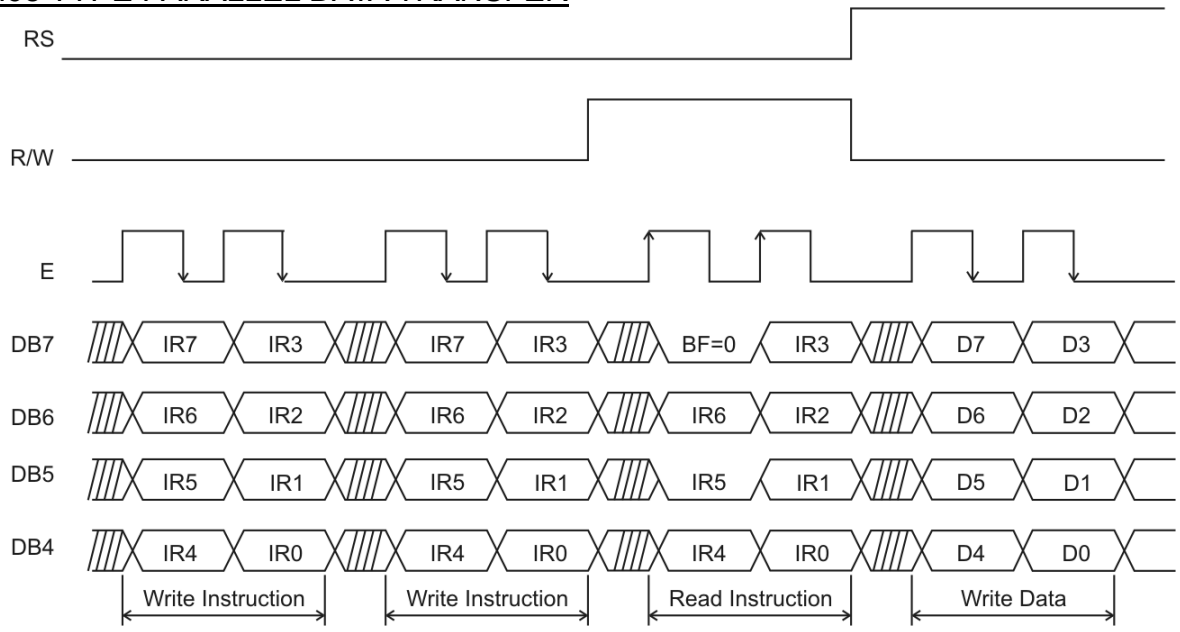
Note:
The cursor or blinking appears when the address counter (AC) selects the Character Generator RAM (CGRAM). The cursor and blinking become meaningless. When the Address Counter is a CGRAM Address, the cursor or the blinking is displayed in a meaningless position.

5.8 CPU INTERFACE (DATA TRANSFER)

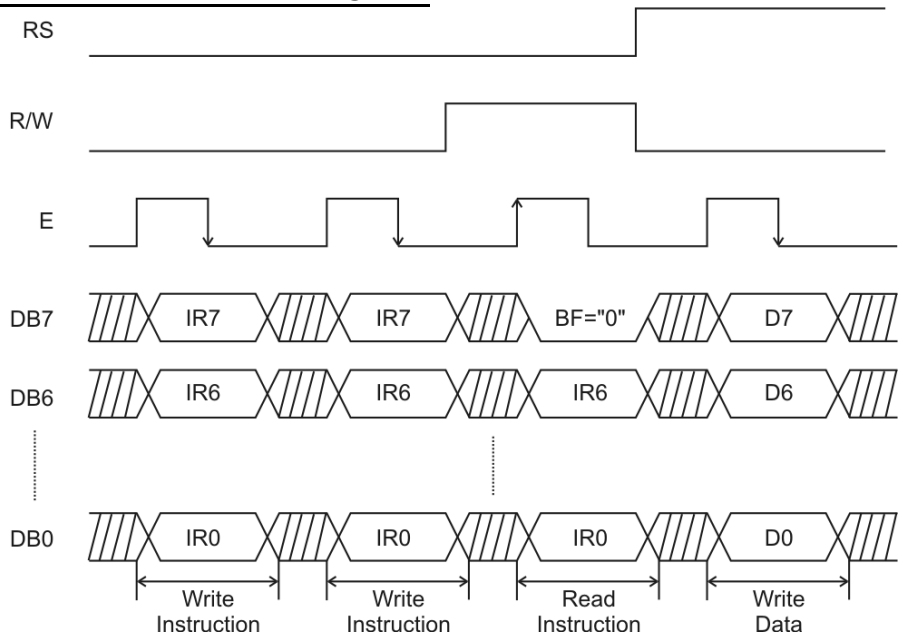
5.8.1 M68 PARALLEL DATA TRANSFER

The M68 type of parallel data transfer is selected when IFSEL is set to “1” and MCU is set to “0” Under this mode, the PT6314 can interface with the CPU in 4 or 8 bits . Please take note that the internal registers are composed of 8 bits. During data transfer in 4 bits, DB4 to DB7 performs the data transfer operation two times, the DB0 to DB3 must be set to either “H” or “L”. The higher order 4 bits (D4 to D7) are initially transferred followed by the lower order 4 bits (D0 toD3). please refer to the diagrams below.

4-BIT M68 TYPE PARALLEL DATA TRANSFER



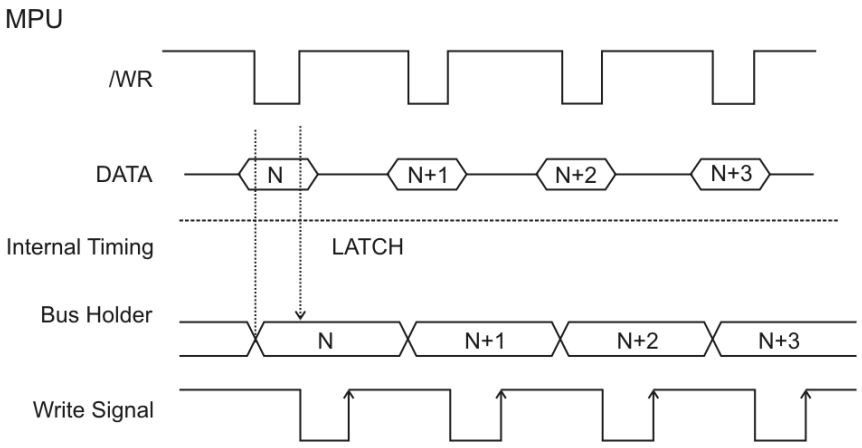
8-BIT M68 TYPE PARALLEL DATA TRANSFER



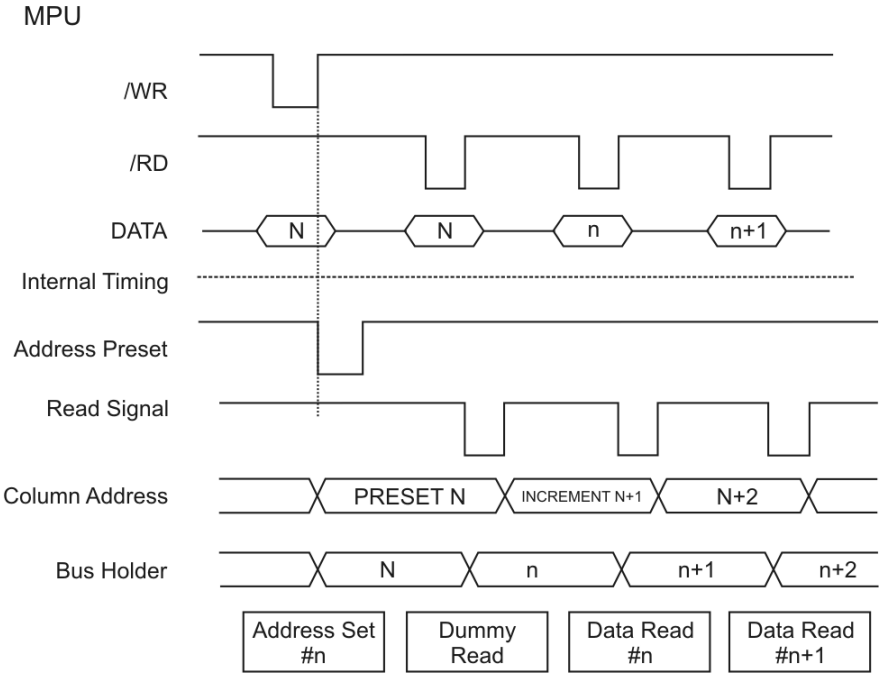
5.8.2 i80 TYPE PARALLEL DATA TRANSFER

The i80 type of parallel data transfer mode is selected when IFSEL is set to “1”and MCU is set to “0”. A type of pipeline process is performed between LSIs via the bus holder attached to the internal data bus whenever data is sent from the MCU. It is important to take note that certain restrictions exists in the read sequence of this display data RAM. The data of the specified address is not generated by the read instructions issued immediately after the address setup. This data is generated in the when the data is read the second time. Thus, a dummy read is required whenever the address setup or write cycle operation is selected. Please refer to the diagrams below.

WRITING



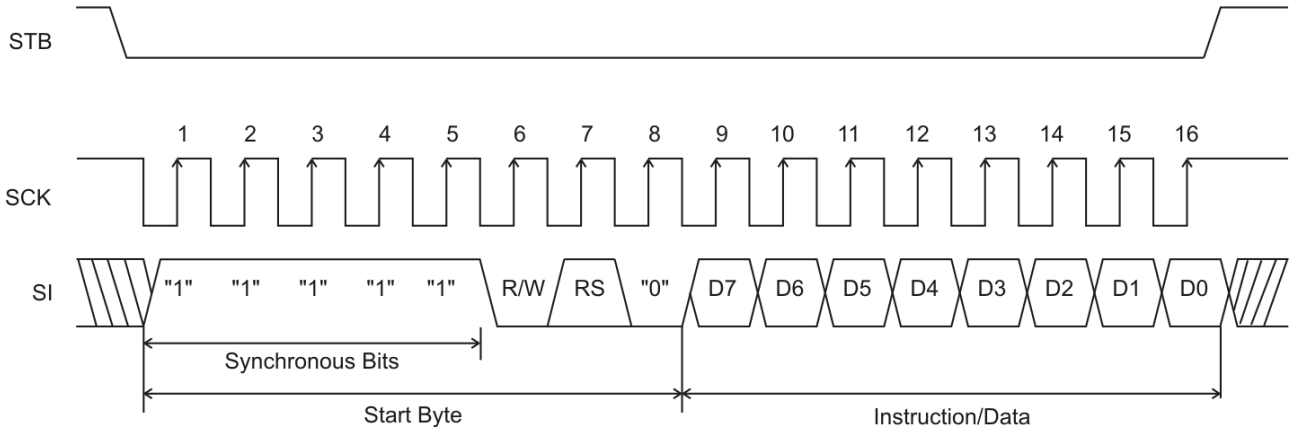
READING



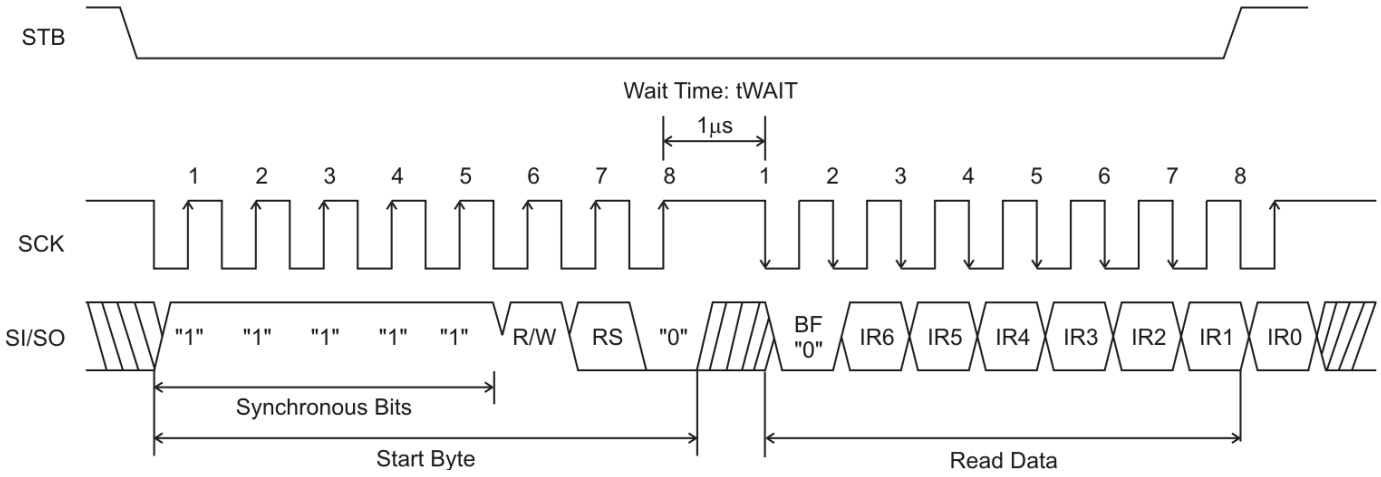
5.8.3 SERIAL DATA TRANSFER

PT6314 supports serial data transfer mode. When data is written, it can be inputted when the Strobe goes to “0”. The first byte -- Start Byte consists of a total of 8 bits: the Synchronous bits (bit 1 - bit 5), R/W (bit 6), RS (bit 7) and bit 8. The register will be selected (IR or DR) by the RS (bit 7) and the data write or read is selected by R/W (bit 6 = “0”) in this byte. The Start Byte is followed by the 8-bit Instruction Byte. The Start Byte selects which is process is to be inputted first: read the Busy Flag + Address Counter (AC6 to AC0) or read the data which was written in the DDRAM or CGRAM. Data is outputted at the falling edge of the shift clock.

DATA WRITE



DATA READ



6. INSTRUCTIONS

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Clear Display	0	0	0	0	0	0	0	0	0	1	Clear all display, and sets DDRAM address at 00H
Cursor Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address at 00H. Also returns the display being shifted to the original position. DDRAM contents remain unchanged.
Entry Mode Set	0	0	0	0	0	0	0	1	1/D	S	Sets the cursor direction and specifies display shift. These operations are performed during the writing/reading of data.
Display ON/Off	0	0	0	0	0	0	1	D	C	B	Sets all display on/off (D) Cursor on/off (C). Cursor blinks on character position (B)
Cursor or Display Shift	0	0	0	0	0	1	SC	R/L	X	X	Shifts display or cursor, also keeps DDRAM contents.
Function Set	0	0	0	0	1	DL	N	X	BR1	BR0	Sets data length (in parallel data transfer) and number of line.
CGRAM Address Set	0	0	0	1	ACG						Sets address of CGRAM. After which CGRAM data is transferred.
DDRAM Address Set	0	0	1	ADD							Sets DDRAM address, after which DDRAM data is transferred.
Read Busy Flag & Address	0	1	BF-="0"	ACC							Reads busy flag (BF) and address counter. BF="0"
Write Data to CGRAM or DDRAM	1	0	Write Data								Writes data into the CGRAM or DDRAM.
Read Data to CGRAM or DDRAM	1	1	Read DR Data								Reads data from CGRAM or DDRAM

Notes:
1. I/D="1": Increment I/D="0": Decrement
2. S="1": Display Shift Enabled S="0": Cursor Shift Enabled
3. D, C, B="1": Turn On D, C, B="0": Turn OFF
4. S/C="1": Display Shift S/C="0": Cursor Shift
5. R/L="1": Shift to the Right R/L="0": Shift to the Left
6. DL="1": 8 Bits DL="0": 4 Bits
7. N="0": 1-Line Display N="1": 2-Line Display
8. BR1, BR0="00": 100% BR1, BR0="10": 50%
   BR1, BR0="01": 75% BR1, BR0="11": 25%
9. X=Irrelevant
10. DDRAM: Display Data RAM
11. CGRAM: Character Generator RAM
12. ACG: CGRAM Address
13. ADD: DDRAM Address
14. ACC: Address Counter

6.1 "CLEAR DISPLAY" INSTRUCTION

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CODE	0	0	0	0	0	0	0	0	0	1

During Reset,

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1

The CLEAR DISPLAY Instruction performs the following operations:
1. Fills all Display Data RAM (DDRAM) location with 20H (Blank Character).
2. Clears the contents of the Address Counter (ACC) to 00H.
3. Sets the display for Zero Character Shift (Returns to original position.)
4. Sets the Address Counter to point to the Display Data RAM (DDRAM).
5. If the cursor is displayed, this instruction will move the cursor to the left most character in the upper display line.
6. Sets the Address Counter (ACC) to increment on each access of the DDRAM or CGRAM.

6.2 "CURSOR HOME" INSTRUCTION

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CODE	0	0	0	0	0	0	0	0	1	X

The CURSOR HOME Instruction performs the following operations:
1. Clears the contents of the Address Counter (ACC) to 00H.
2. Sets the Address Counter to point to the Display Data RAM (DDRAM).
3. Sets the Display for Zero Character Shift (Returns to the original position).
4. If the cursor is displayed, this instruction moves the cursor to the left most character in the upper line display.

6.3 "ENTRY MODE" INSTRUCTION

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CODE	0	0	0	0	0	0	0	01	1/D	S

The "I/D" Bit provides a way to modify the contents of the address counter after every access to the DDRAM or CGRAM. When I/D is set to "1" the Address Counter is incremented after the DDRAM or CGRAM has been accessed. When the I/D is set to "0" the Address Counter is decremented after the DDRAM or CGRAM has been accessed.

The "S" Bit controls the display or cursor shift after each read or write operation to the DDRAM. If S is set to "1" the "Display Shift" Instruction is enabled. If the S is set to "0" the "Cursor Shift" Instruction is enabled.

The direction in which the display is shifted is opposite to that of the cursor. For example, if S="0" and I/D="1" the cursor will shift one character to the right after the MCU writes to the DDRAM. But, if the S="1" and I/D="1" the display will shift one character to the left and the cursor will remain in the same position in the panel display. The cursor has already been shifted in the direction selected by the I/D during the reading of the DDRAM irrespective of the value of "S". Reading and writing the CGRAM always shifts the cursor. Both lines are shifted at the same time.

The table below shows the various cursor and display shift movements by the "Entry Mode Set".

I/D	S	After Writing DDRAM Data	After Reading DDRAM Data
0	0	Cursor moves one character to the left.	Cursor moves one character to the left.
1	0	Cursor moves one character to the right.	Cursor moves one character to the right.
0	1	Display shifts one character to the right without any cursor movement.	Cursor moves one character to the left.
1	1	Display shifts one character to the left without any cursor movement.	Cursor moves one character to the right.

During Reset,

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0

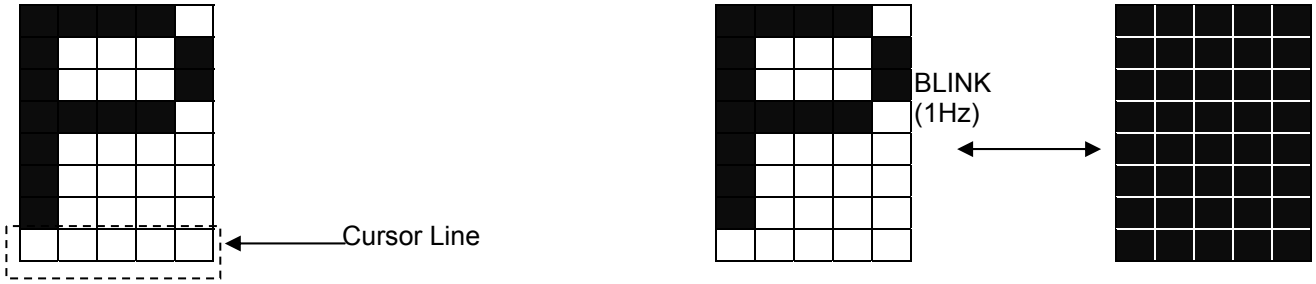
6.4 "DISPLAY ON/OFF" INSTRUCTION

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CODE	0	0	0	0	0	0	1	D	C	B

The above instruction controls the various display features:

D="1": Display ON D="0": Display OFF
C="1": Cursor ON C="0": Cursor OFF
B="1": Blinking ON B="0": Blinking OFF

Blinking is achieved by alternating a normal and an all "ON" display of a character. The cursor blinks with a frequency of approximately 1 Hz and 50% duty.



During Reset,

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	0

6.5 "CURSOR OR DISPLAY SHIFT" INSTRUCTION

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CODE	0	0	0	0	0	1	S/C	R/L	X	X

The instruction above will shift the display and/or move the cursor one character to the left or right, without DDRAM reading or writing.

"S/C" Bit selects between the movement of both cursor and display or the movement of the cursor alone. When "S/C"="1" the cursor and the display are both shifted. When "S/C"="0" only the cursor is shifted.

The "R/L" Bit selects the left or right movement direction of the cursor and/or display. When "R/L"="1" the cursor and/or display is shifted one character to the right. When "R/L" is "0" the cursor and/or character is shifted to the left.

The table below summarizes display and cursor shift and movement.

S/C	R/L	Cursor	Display
0	0	Move one character to the left.	No shift
0	1	Move one character to the right.	No shift
1	0	Move one character to the left with display	Shift one character to the left.
1	1	Move one character to the right with display	Shift one character to the right.

6.6 "FUNCTION SET" INSTRUCTION

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CODE	0	0	0	0	1	DL	N	X	BR1	BR0

The instruction above sets the data length of the data bus lines. This instruction initializes the system, and must be the first instructed executed after power is turned ON.

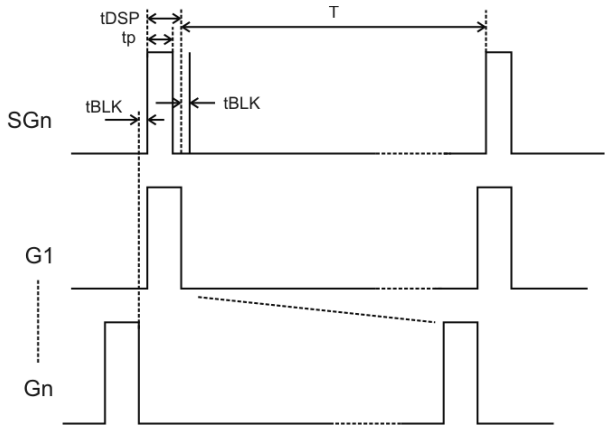
The "DL" and "N" settings are described below:

"DL"="1": 8-bit MCU Interface using DB7 to DB0
"DL"="0": 4-bit MCU Interface using DB7 to DB4
"N"="0": 1-Line Display using SG1 to SG40. (SG41 to SG80 are fixed at "Low Level")
"N"="1":2-Line Display using SG1 to SG80
x = Not Relevant

BR1 and BR0 flags are used to modulate the pulse width of the Segment Output thereby controlling the VFD brightness.

BR1	BR0	Brightness	tp
0	0	100%	tDSP x 1.00
0	1	75%	tDSP x 0.75
1	0	50%	tDSP x 0.5
1	1	25%	tDSP x 0.25

tDSP≒200μs, tBLK≒10μs



where n = number of Grid, T =n x (tDSP + tBLK)

During Reset,

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0

6.7 "CGRAM ADDRESS SET" INSTRUCTION

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CODE	0	0	0	1	A	A	A	A	A	A

The above instruction is used to (1) load new 6-bit address into the address counter, and (2) set the address counter to point to the CGRAM.

Once the "CGRAM Address Set" instructions has been executed, the contents of the address counter (ACC) is automatically modified after every access of the CGRAM, as determined by the "Entry Mode Set" instruction. The active width of the address counter, when it is addressing the CGRAM is 6 bits. The counter will wrap around from 00H to 3FH if more than 64 bytes of data is written to the CGRAM.
During Reset, this instruction is irrelevant.

6.8 "DDRAM ADDRESS SET" INSTRUCTION

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CODE	0	0	1	A	A	A	A	A	A	A

The above instruction is used to (1) load new 7 bits address into the address counter, and (2) set the address counter to point to the CGRAM.

Once the "DDRAM Address Set" instruction has been executed, the contents of the address counter (ACC) is automatically modified after every access of the DDRAM, as determined by the "Entry Mode Set" instruction. The valid DDRAM address range is given below.

Line Display	Number of Characters	Address Range
1st Line	40	00H to 27H
2nd Line	40	40H to 67H

During Reset, this instruction is irrelevant.

6.9 "READ BUSY FLAG AND ADDRESS" INSTRUCTION

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CODE	0	1	BF	A	A	A	A	A	A	A

The above instruction reads the Busy Flag (BF) * and the value of the address counter in binary "AAAAAAA". This address counter is used by the CGRAM and DDRAM addresses and its values are determined by the previous instruction. Address counter contents are the same as that of "CGRAM Address Set" and "DDRAM Address Set" Instructions.

Note: * The Busy Flag (BF) = "0"

6.10 "WRITE DATA TO CGRAM OR DDRAM" INSTRUCTION

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CODE	1	0	D	D	D	D	D	A	D	D
			←High Order Bit						Low Order Bit→	

The above instruction write 8 bits binary data "DDDDDDDD" to the CGRAM or DDRAM.
Writing into the CGRAM or DDRAM is determined by the previous instruction of the "CGRAM or DDRAM Address Set". After a data is written, the value of the address is automatically increased or decreased by one in accordance to the selection made by the "Entry Mode Set". The "Entry Mode Set" also determines the display shift.

6.11 "READ DATA FROM CGRAM OR DDRAM" INSTRUCTION

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CODE	1	1	D	D	D	D	D	A	D	D
			←High Order Bit							Low Order Bit→

The above instruction reads the 8 bits binary data "DDDDDDDD" from the CGRAM or DDRAM. The "CGRAM or DDRAM Address Set" instruction must be executed first before this instruction can be entered. If the "CGRAM or DDRAM Address Set" is not executed prior to the "READ Data from CGRAM or DDRAM" then the first READ data becomes invalid. When "Read" Instructions are serially executed, the next address data is normally read from the second "Read". Before the cursor shifts by the "Cursor or Display Shift" Instruction, the address set instruction do not need to be executed before the read instruction (only applies to DDRAM). The operation of the cursor shift instruction is the same as the "DDRAM Address Set" Instruction.

After reading one data, the value of the address is automatically increased or decreased by 1 in accordance to the selection made in the "Entry Mode". Please note that the address counter is automatically increased or decreased by 1 after "Write Data to CGRAM or DDRAM" Instruction is executed. At this moment, the address counter's target data cannot be read if the "Read Data from CGRAM or DDRAM" Instruction is executed. Thus, to read data correctly, the "Address Set" or "Cursor Shift" (if Read Data from DDRAM only) Instruction must be executed before reading.

6.12 POWER ON RESET

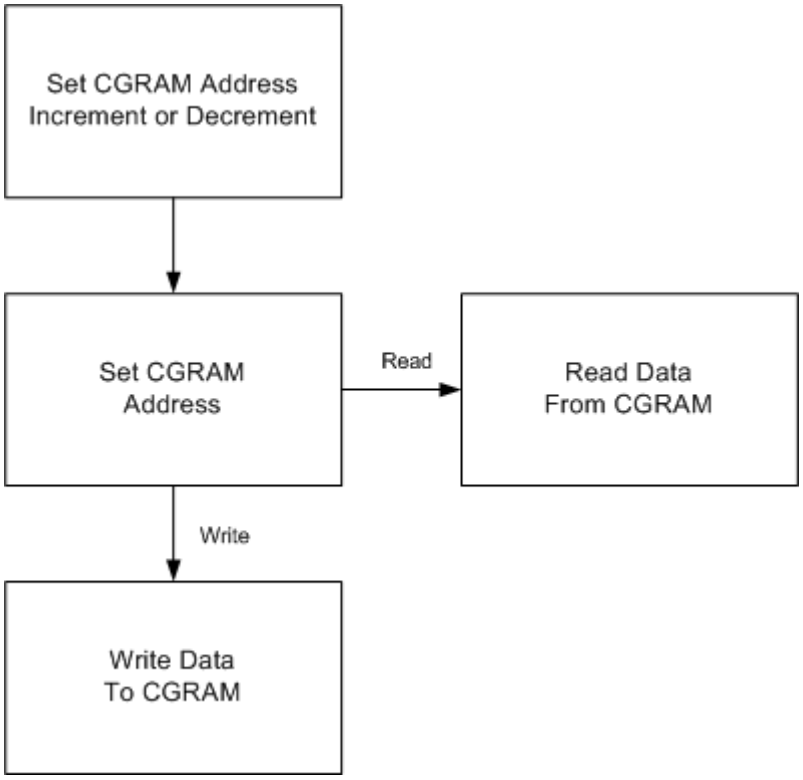
When PT6314 is initialized, the internal status after power supply has been reset is as follows:
1. Display Clear: 20H (space code) fills the DDRAM
2. Address Counter is set to 00H
3. Address Counter is pointed to the DDRAM
4. Display ON/OFF: D=0, C=0, B=0 (Display OFF)
5. Entry Mode Set: I/D=1, S=0 (Increment, Cursor Shifts are enabled)
6. Function Set: DL=1, N=1 (8-Bit MCU Interface, 2-Line Display are enabled.)
7. Brightness Control: BR0=BR1=0 (Brightness = 100%)

For the MCU Interface and Duty Ratio Selection, please refer to the table below.

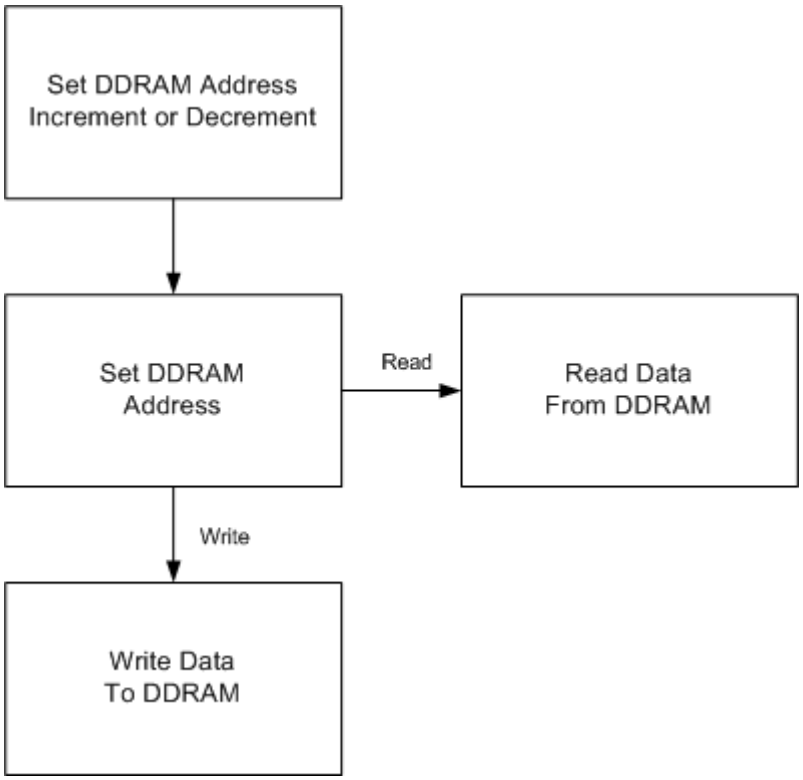
Pin Name				Function	Remarks
TEST	IFSEL	DS1	DS0		
0	X	X	X	Self Test Mode	This is effective specially after long usage.
1	0	X	X	Serial Interface	SI/SO, SCK, STB
1	1	X	X	Parallel Interface	RS, E, R/W, DB7 to DB4 or DB7 to DB0
1	X	0	0	Duty=1/16(16Cx1 or 2L Display)	It does not need to use the extension driver. The number of display lines is selected by instruction.
1	X	0	1	Duty=1/20(20Cx1 or 2L Display)	
1	X	1	0	Duty=1/24(24Cx1 or 2L Display)	
1	X	1	1	Duty=1/40(40Cx1 or 2L Display)	Extension driver must be used. The number of display lines is selected by instruction.

The above table shows the relationship between the status of PT6314 and the pin states during RESET.

6.13 CGRAM STROKE FLOWCHART



6.14 DDRAM STROKE FLOWCHART



7. ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=+25℃, Vss1=Vss2=0V)

Parameter		Symbol	Rating	Unit
Logic power supply voltage		VDD1	-0.5 to +6.0	V
Logic input voltage		Vi	-0.5 to VDD1 + 0.5	V
Logic output voltage		Vo	-0.5 to VDD1 +0.5	V
Driver power supply voltage		VDD2	-0.5 to +60	V
Driver output voltage		VO2	-0.5 to VDD2 + 0.5	V
Driver output current	Segment	IOL2S	+10	mA
		IOH2S	-4	mA
	Grid	IOL2G	+10	mA
		IOH2G	-20	mA
Power dissipation		PD	1.2	W
Operating temperature		Topr	-40 to +85	℃
Storage temperature		Tstg	-65 to +150	℃

8. RECOMMENDED OPERATING RANGE

(Unless otherwise specified, Ta=+25℃, Vss1=Vss2=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Logic power supply voltage		VDD1	4.5	5.0	5.5	V
Logic system input voltage		VIN	0	-	VDD1	V
Driver power supply voltage		VDD2	20	-	50	V
Drive output current	Segment	IOL2S	-	-	+5	mA
		IOH2S	-	-	-2	mA
	Grid	IOL2G	-	-	+5	mA
		IOH2G	-	-	-15	mA

Note: It is recommended that the order in which power is to be applied to the chipset is as follows: VDD1 → Input → VDD2

9. ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=-40 to +85℃, VDD1=5.0V, VDD2=50V, VSS1=VSS2=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage 1	VIH1	Logic, Expect E/SCK,RESET	0.7VDD1	-	-	V
Low level input voltage 1	VIL1	Logic, Expect E/SCK,RESET, DLS	-	-	0.3 VDD1	V
High level input voltage 2	VIH2	E/SCK, RESET	0.8VDD1	-	-	V
Low level input voltage 2	VIL2	E/SCK, RESET,DLS	-	-	0.2 VDD1	V
High level output voltage (LOGIC)	VOH1	DBn, SI/SO, SDO, SLK, LATCH,/CLR, IOH1=-0.1mA	VDD1-0.5	-	-	V
Low level output voltage (LOGIC)	VOL1	DBn, SI/SO, SDO, SLK, LATCH,/CLR, IOL1=+0.1mA	-	-	VSS1+0.5	V
High level input current	IIH	TEST, VIN=VDD1	20	-	500	μA
High level leakage current	ILOH	Logic, VINOUT=VDD1	-	-	1.0	μA
Low level leakage current	ILOL	Logic, VINOUT=VSS1	-	-	-1.0	μA
High level output voltage (DRIVER)	VOH2S1	SG1to SG80, IOH2=-1mA	46	-	-	V
	VOH2S2	SG1 to SG80, IOH2=-2mA	45	-	-	V
	VOH2G	GR1 to GR24, IOL2=-15mA	45	-	-	V
Low level output voltage (DRIVER)	VOL2	SG1 to SG80, GR1 to GR24 IOL2=1mA	-	-	5	V
Current consumption	IDD1	Logic	-	-	100	μA
	IDD2	Driver	-	-	100	μA

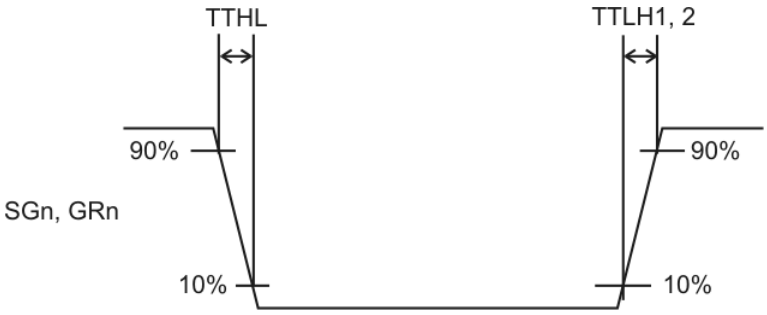
Note: The Typical (Typ.) Value is a reference value when Ta=25℃.

10. SWITCHING CHARACTERISTICS

(Unless otherwise specified, Ta=-40 to +85℃, VDD1=5.0 ±10%)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	Fosc	R=56KΩ	392	560	728	KHz
Operation frequency	fc	OSC1 External Clock	450	560	900	KHz
Rise time	TTLH1	SG1 to SG80, CL=50pF	-	-	2.0	μs
Rise time	TTLH2	GR1 to GR24, CL=50pF	-	-	2.0	μs
Fall time	TTHL	SG1 to SG80, GR1 to GR24m, CL=50pF	-	-	2.0	μs

11. SWITCHING TIMING



11.1 TIMING 1 REQUIREMENTS

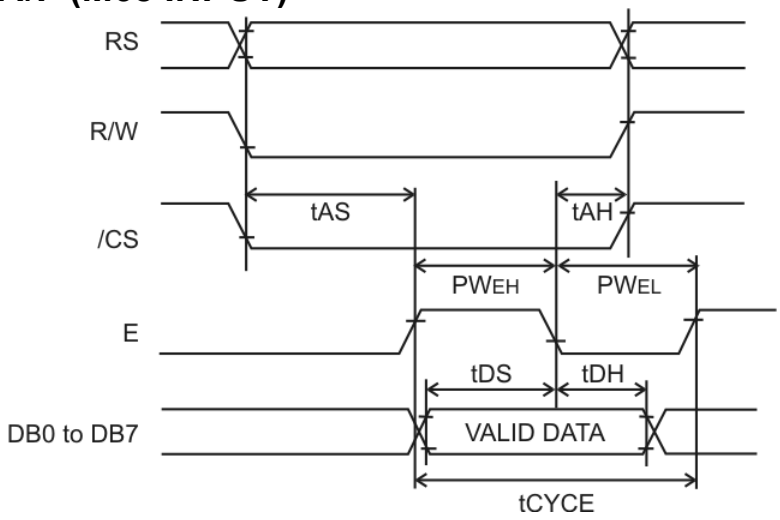
(Unless otherwise specified, Ta=-40 to +85℃); M68 Interface Parallel Data Transfer: Write (VDD1=5.0V ±10%)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Enable cycle time	tCYCE	E ↑ → E ↑	500	-	-	ns
Enable “H” pulse width	PWEH	E	230	-	-	ns
Enable ”L” pulse width	PWEL	E	230	-	-	ns
RS, R/W - E setup time	tAS	RS,R/W → E ↑	20	-	-	ns
RS, R/W - E hold time	tAH	E ↓ → RS,R/W	10	-	-	ns
Data setup time	tDS	Data → E ↓	80	-	-	ns
Data hold time	tDH	E ↓ → Data	10	-	-	ns
Reset pulse width	tWRE		500	-	-	ns

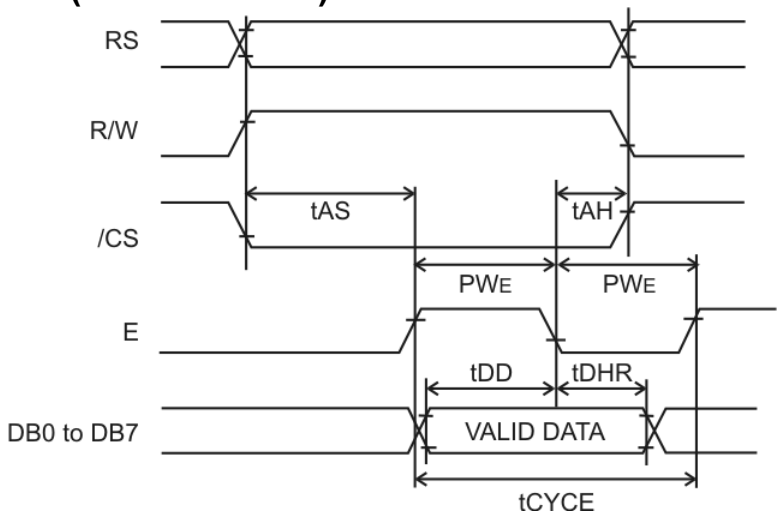
M68 Interface Parallel Data Transfer: Read (VDD1=5.0±10%)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Enable cycle time	tCYCE	E ↑ → E ↑	500	-	-	ns
Enable “H” pulse width	PWEH	E	230	-	-	ns
Enable ”L” pulse width	PWEL	E	230	-	-	ns
RS, R/W - E setup time	tAS	RS,R/W → E ↑	20	-	-	ns
RS, R/W - E hold time	tAH	E ↓ → RS,R/W	10	-	-	ns
Data delay time	tDD	E ↑ → Data	-	-	160	ns
Data hold time	tDHR	E ↓ → Data	5	-	-	ns

11.1.1 PARALLEL I/F (M68 INPUT)



11.1.2 PARALLEL I/F (M68 OUTPUT)



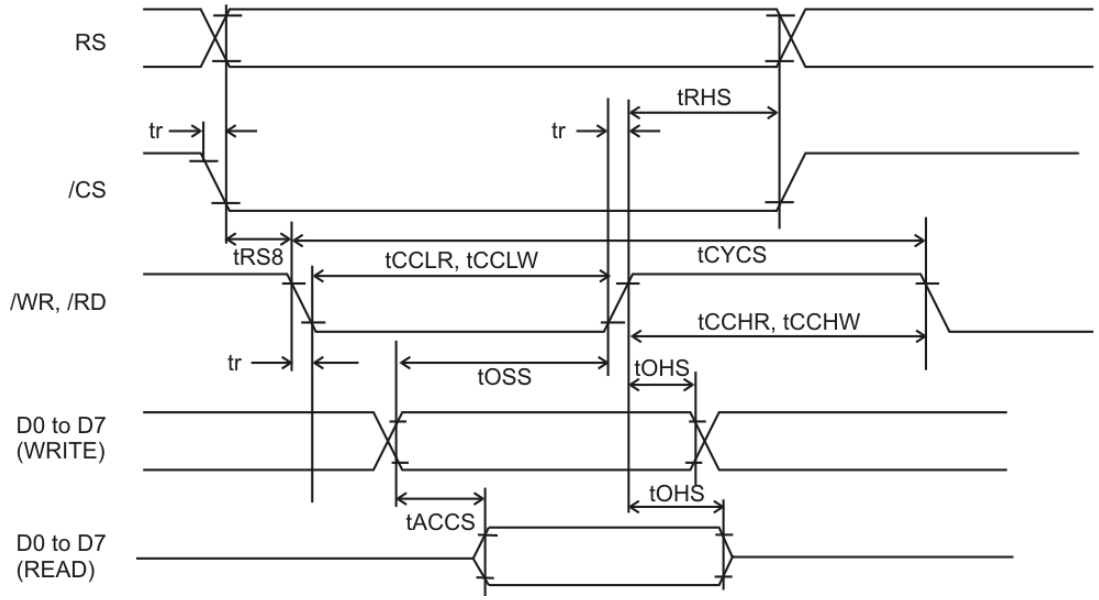
Notes:
1. Input Signal Rise Time and Fall Time (tF, tR) < 15ns.
2. All timing is specified using 0.20VDD1 and 0.80VDD1 as reference.
3. PWEH is the overlap between /CS="L" and E.

11.2 TIMING 2 REQUIREMENTS

(Unless otherwise specified, Ta=-40 To +85℃);i80 Interface Parallel Data Transfer: Write (VDD1=5.0 ±10%)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
RS hold time	tRH8		10	-	-	ns
RS setup time	tRS8		10	-	-	ns
System cycle time	tCYC8		168	-	-	ns
Control “L” pulse width (WR)	tCCLW	/WR	30	-	-	ns
Control “L” pulse width (RD)	tCCLR	/RD	70	-	-	ns
Control “H” pulse width (RD)	tCCHW	/WR	100	-	-	ns
Control “H” pulse width (RD)	tCCHR	/RD	70	-	-	ns
Data setup time	tDS8	D0 to D7	55	-	-	ns
Data hold time	tDH8	Do to D7	55	-	-	ns
RD access time	tACC8	Do to D7, CL=100pF	-	-	70	ns
Output disable time	tOH8	Do to D7, CL=100pF	5	-	-	ns
Reset pulse width	tWRE		500	-	-	ns

11.2.1 PARALLEL I/F (i80)



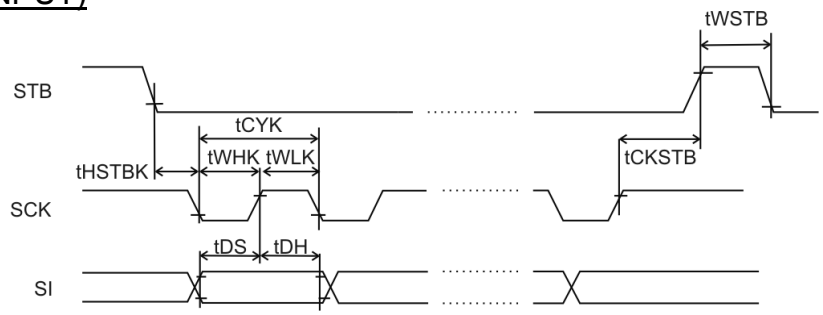
Notes:
1. Input signal rise time and fall time (tF, tR) < 15ns
2. All timing is specified using 0.20VDD1 and 0.80VDD1 as reference.
3. tCCLW and tCCLR are specified as the overlap between /CS=”L” /WR and /RD=”L”

11.3 TIMING 3 REQUIREMENTS

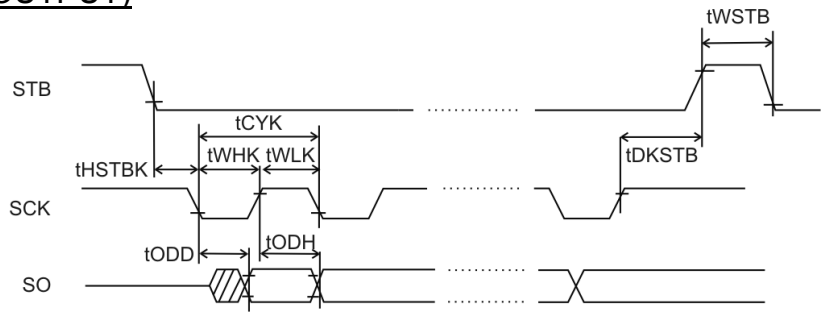
(Unless otherwise specified, Ta=-40 to +85℃); Serial Data Transfer: (VDD1=5V±10%)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock cycle	tCYK	SCK	500	-	-	ns
High level shift clock pulse width	tWHK	SCK	200	-	-	ns
Low level shift clock pulse width	tWLK	SCK	200	-	-	ns
Shift clock hold time	tHSTBK	STB↓ → SCK↓	100	-	-	ns
Data setup time	tDS	Data → SCK↑	100	-	-	ns
Data hold time	tDH	SCK↑ → Data	100	-	-	ns
STB hold time	tDKSTB	SCK↑ → STB↑	500	-	-	ns
STB pulse width	tWSTB		500	-	-	ns
Wait time	tWAIT	8th CLK↑→ 1st CLK↓	1	-	-	ns
Output data delay time	tODD	SCK↓ → Data	-	-	150	ns
Output data hold time	tODH	SCK↑ → Data	5	-	-	ns
Reset pulse width	tWRE		500	-	-	ns

11.3.1SERIAL I/F (INPUT)

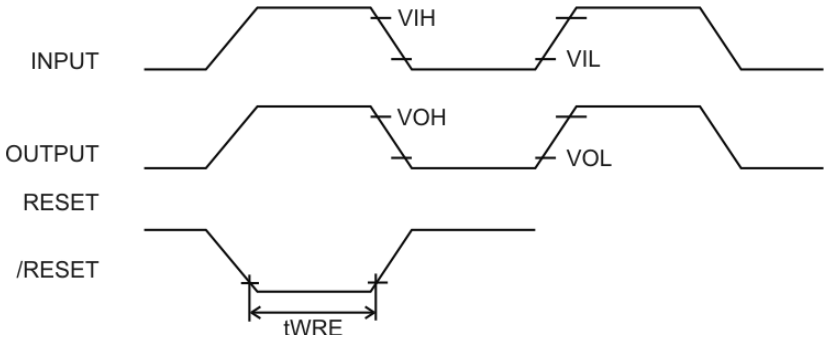


11.3.2 SERIAL I/F (OUTPUT)



Notes:
1. Input Signal Rise Time and Fall Time (tF, tR) < 15 ns.
2. All timing is specified using 0.20VDD1 and 0.80VDD1 as reference.

11.3.3 AC MEASUREMENT POINT

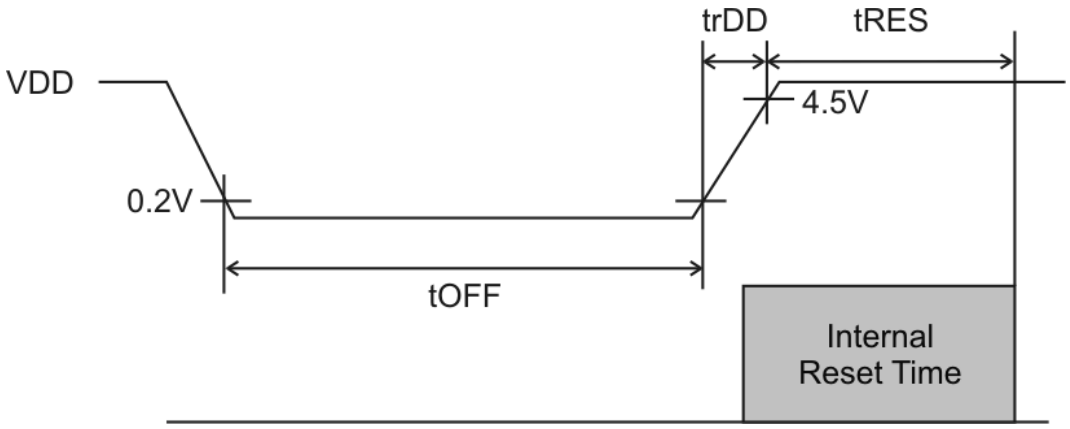


11.4 TIMING 4 REQUIREMENTS

(Unless otherwise specified, Ta=-40 to +85℃)

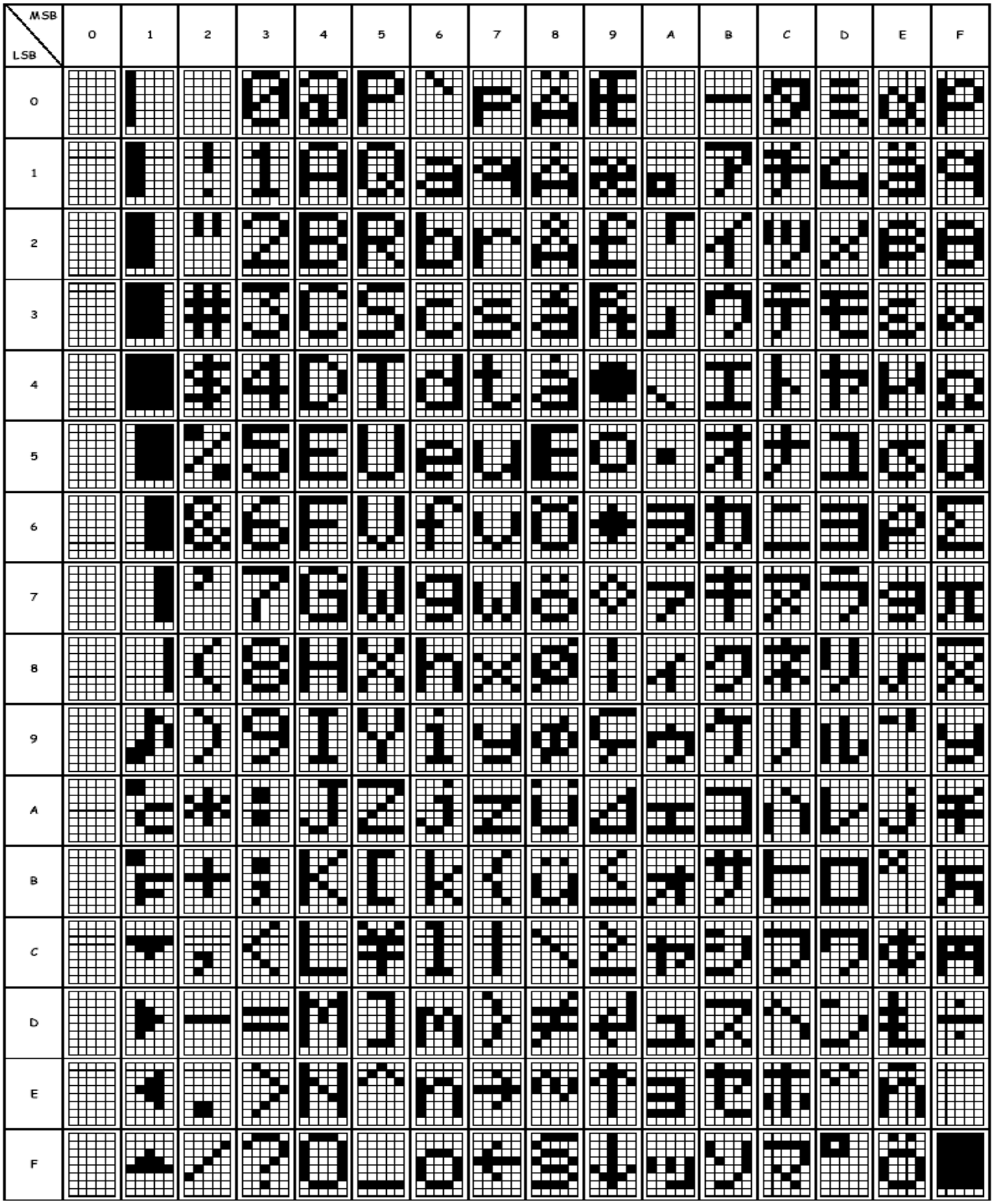
M68 & i80 Serial Interface Common Timing: Power ON RESET (VDD1=5.0±10%)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time	tRES	VDD	100	-	-	μs
VDD rising time	trDD	VDD	1	-	-	μs
VDD off width	tOFF	VDD	1	-	-	ms

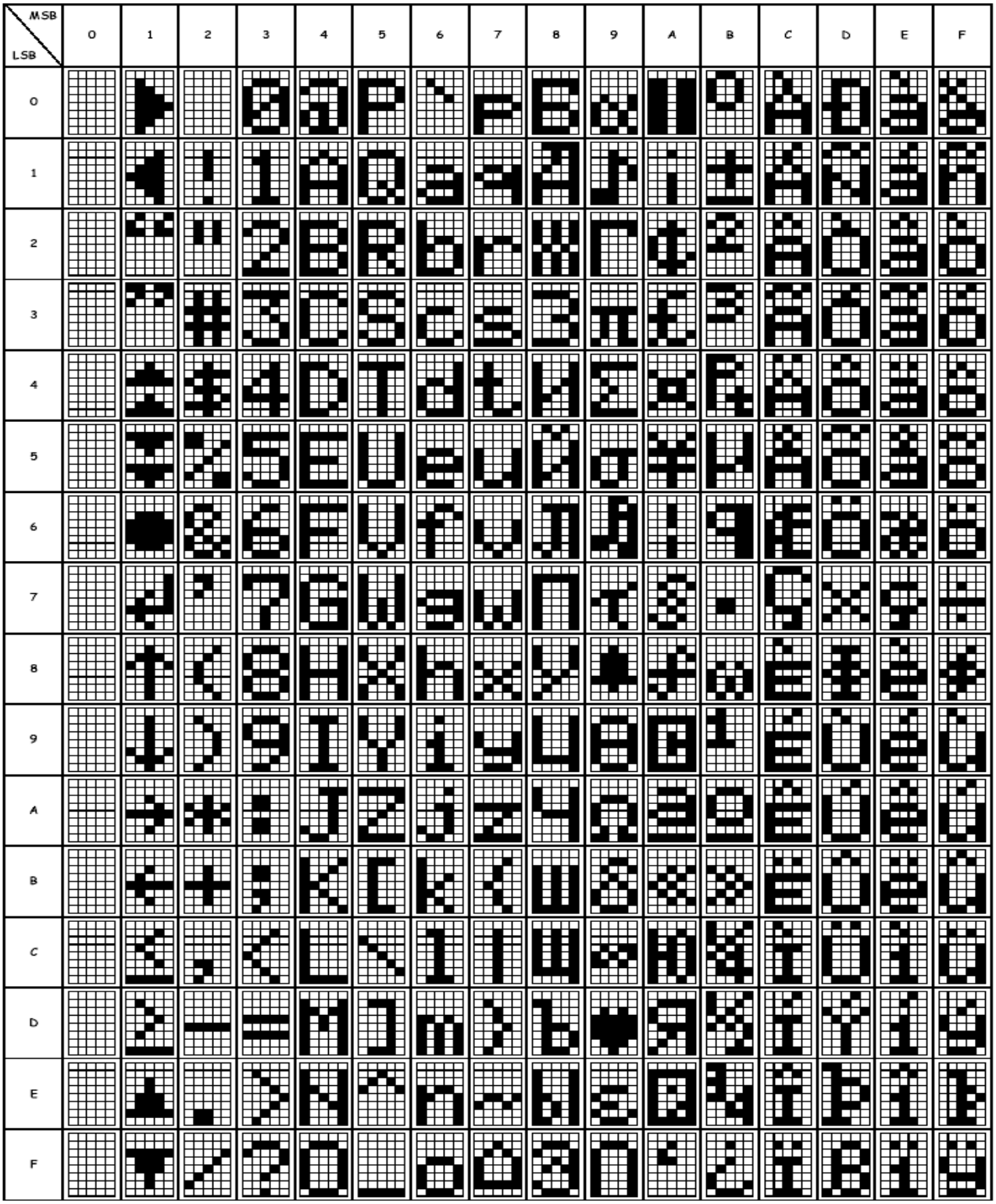


12. FONT TABLE

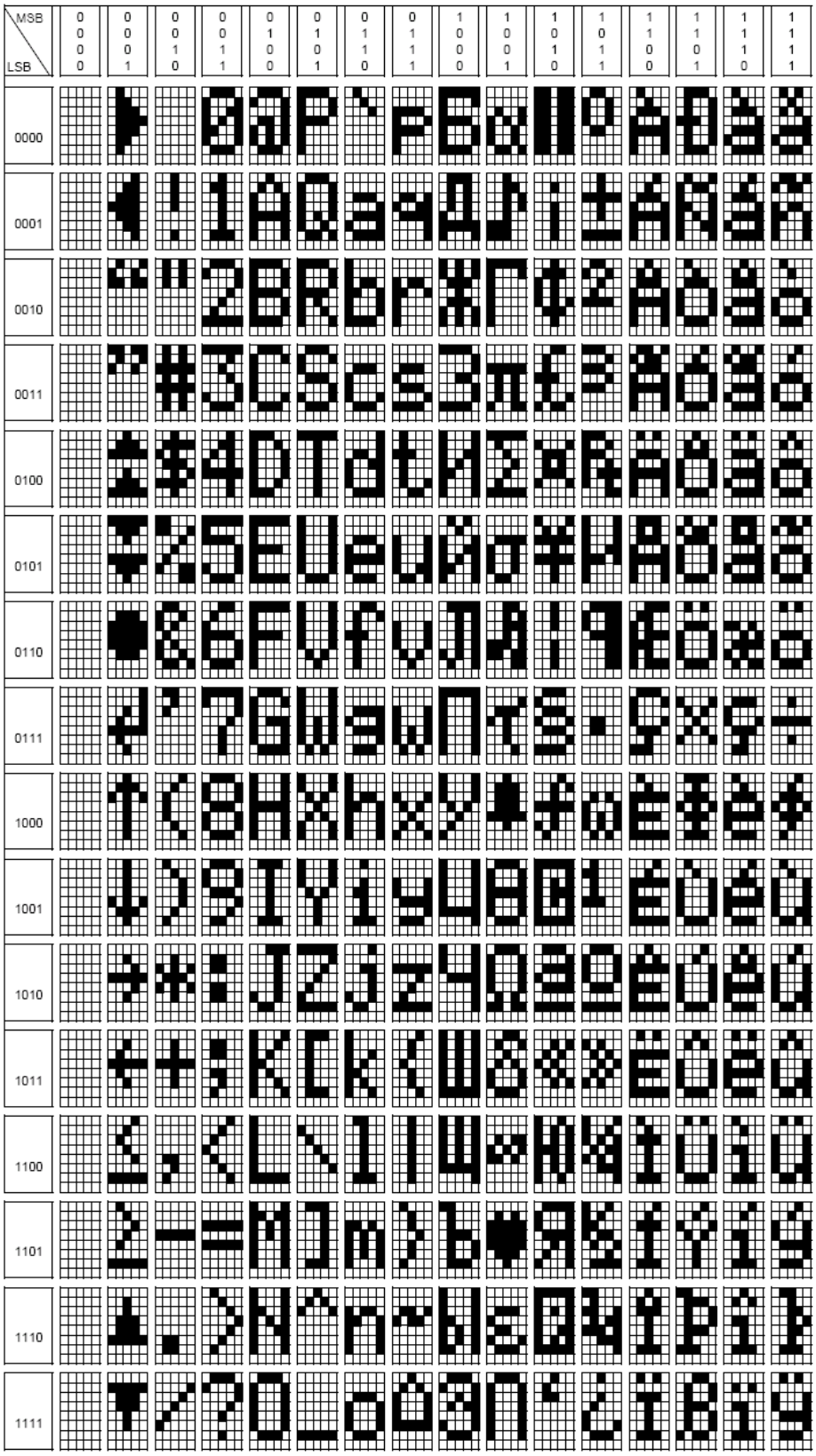
12.1 ENGLISH/JAPANESE CHARACTER FONT TABLE (PT6314-001)



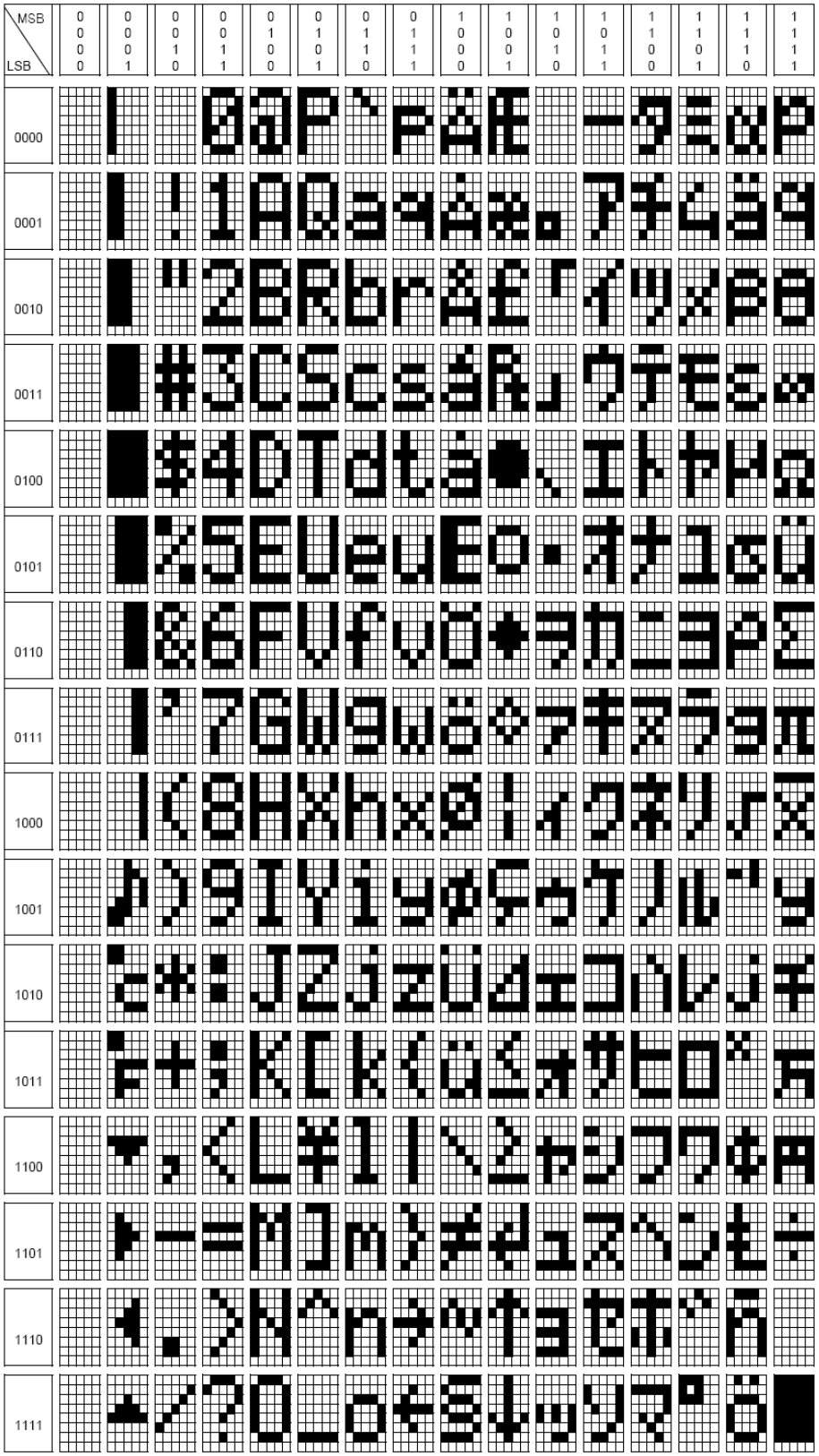
12.2 ENGLISH/EUROPEAN CHARACTER FONT TABLE (PT6314-002)



12.3 EUROPEAN CHARACTER FONT TABLE (PT6314-007)

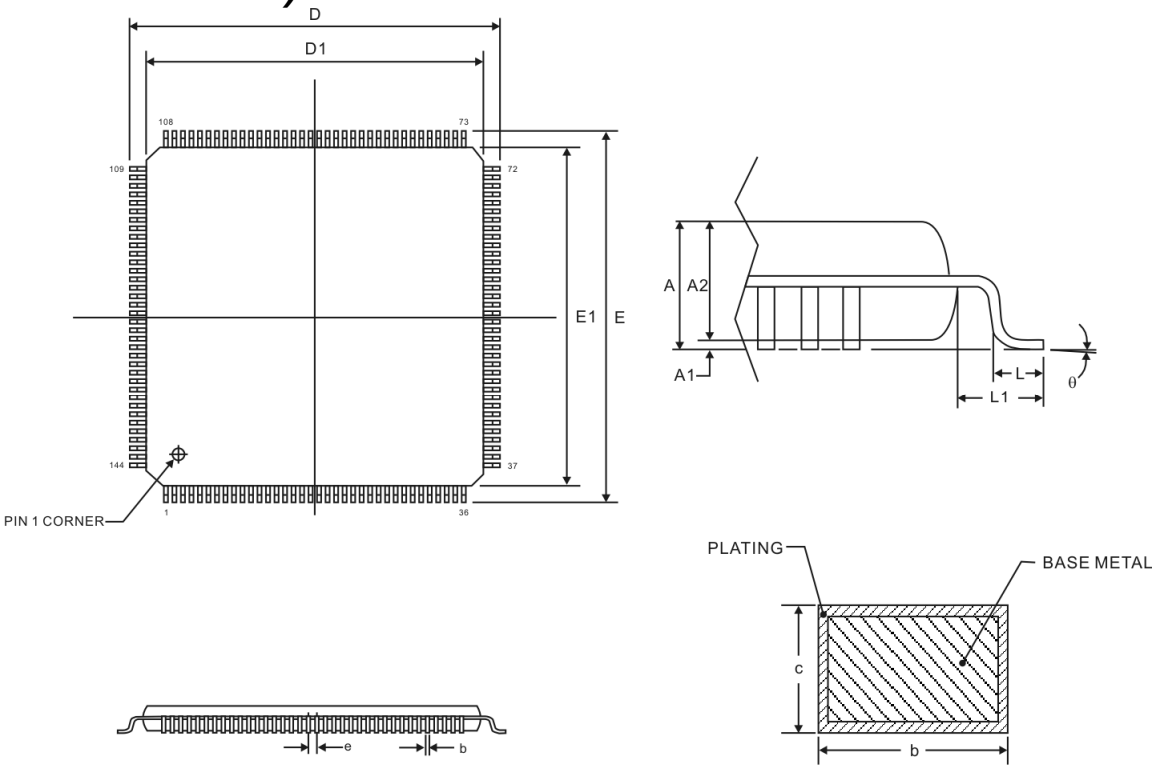


12.4 JAPANESE CHARACTER FONT TABLE (PT6314-008)



13. PACKAGE INFORMATION

144 Pins, LQFP (BODY SIZE: 20 X 20MM, PITCH SIZE: 0.50mm, THK BODY: 1.40mm)



Symbol	Min.	Nom.	Max.
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	1.4	1.45
b	0.17	0.22	0.27
c	0.09	-	0.2
D	22 BSC.		
D1	20 BSC.		
e	0.5 BSC.		
E	22 BSC.		
E1	20 BSC.		
L	0.45	0.6	0.75
L1	1 REF.		
θ	0°	3.5°	7°

Notes:
1. Refer to JEDEC MS-026
2. All dimensions are in millimeter.

IMPORTANT NOTICE

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