## DOT MATRIX LCD CONTROLLER & DRIVER

KS0072 is a dot matrix LCD driver & controller LSI which is fabricated by low power CMOS technology. It is capable of displaying 1 line 16 characters or 2 line 8 characters with 5 X 8 dots format.

## FUNCTIONS

Character type dot matrix LCD driver & controller.

- Easy interface with 4-bit or 8-bit MPU.
- Internal driver : 16 common and 40 segment signal output.
- Display character pattern : 5 X 8 dots format (240 kinds)
- Direct programming of the special charactor patherns by character Generator RAM.
- Mask open for programming customer charactor patterns
- Various instruction functions.
- Automatic power on reset.

## FEATURES

Internal Memory

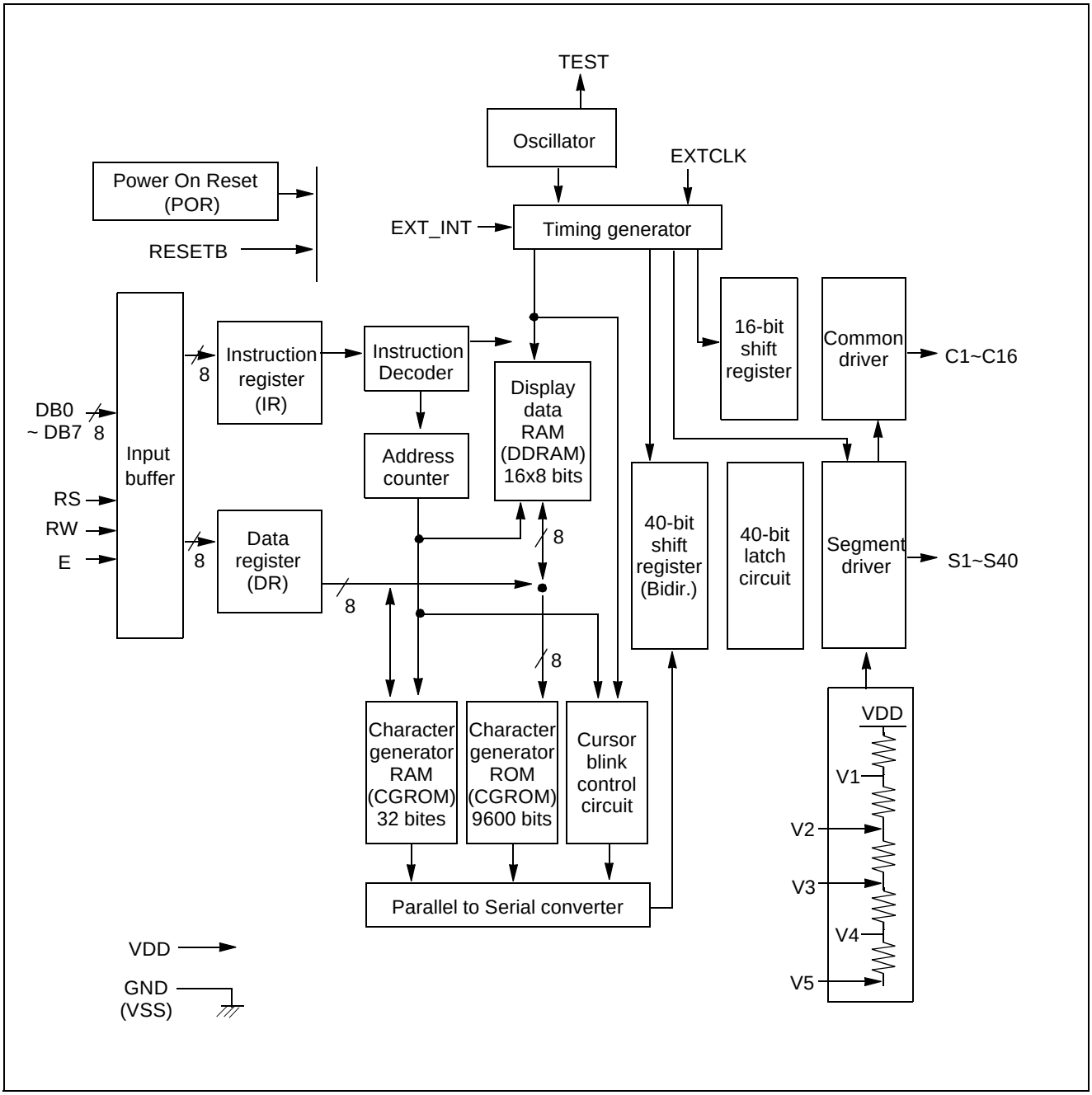
- Character Generator ROM (CGROM) :9600bits (240 characters X 5 X 8 dot)
- Character Generator RAM (CGRAM) : 160 bits (4 characterX5X8 dot)
- Display Data RAM (DDRAM) : 128bits(16 charactersX8bits)

- Low power operation

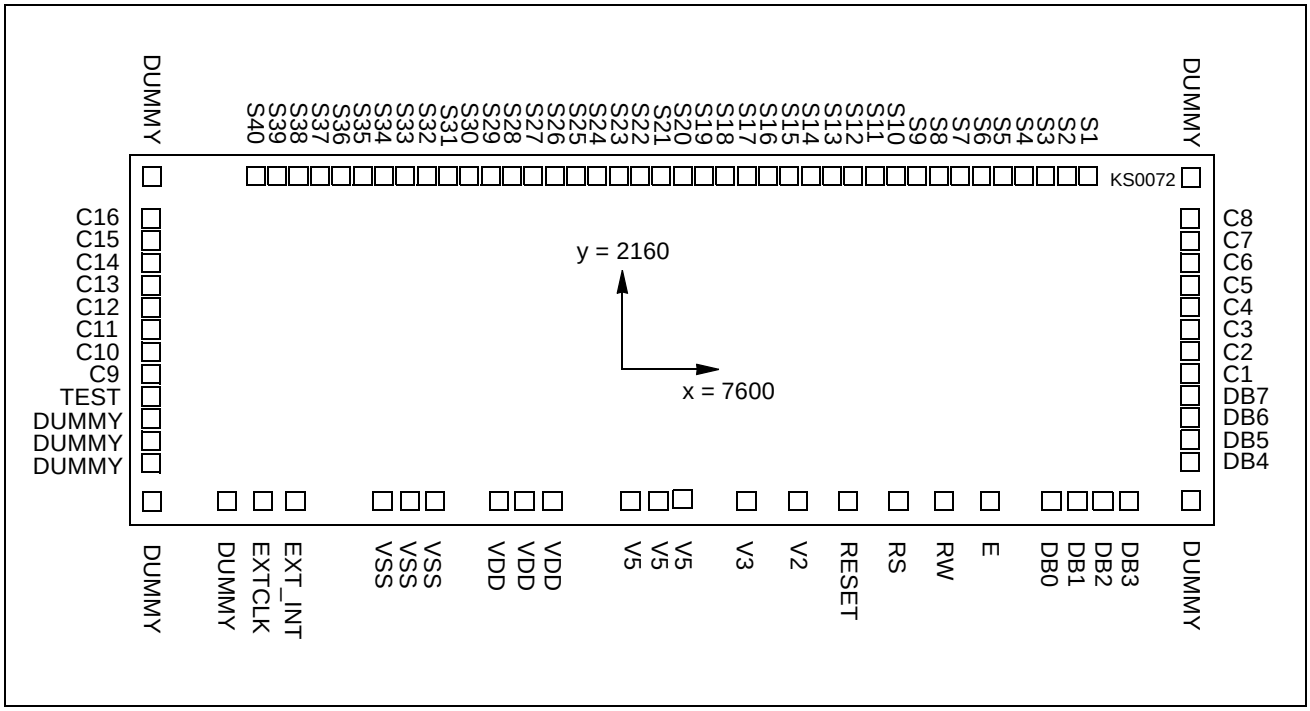
- Power supply voltage range : 2.7 ~ 5.5V(VDD)
- LCD drive voltage range : 3.0 ~ 11.0(VDD-V5)

- CMOS process
- Duty cycle : 1/16
- Built-in oscillator
- Low power consumption
- Internal divide resistor for LCD driving voltage
- Available for COG

## BLOCK DIAGRAM



## PAD DIAGRAM




KS0072

CHIP SIZE : 7600 X 2160㎛
PAD PITCH : min. 125㎛
CHIP THICKNESS : 675㎛

1) AL PAD SPECIFICATIONS

AL PAD SIZE ON Y SIDE : 87 X 94㎛
AL PAD SIZE ON X SIDE : 94 X 87㎛

2) AU BUMP SPECIFICATIONS

BUMP SIZE ON Y SIDE : 77 X 84 ㎛
BUMP SIZE ON X SIDE : 84 X 77㎛
BUMP HEIGHT : 18 $\pm$ 3 ㎛ (for reference)

## PAD LOCATION

| NO | NAME | X | Y | NO | NAME | X | Y | NO | NAME | X | Y |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | DUMMY | -3642 | -881 | 31 | C3 | 3643 | 64 | 61 | S24 | -455 | 923 |
| 2 | DUMMY | -3032 | -881 | 32 | C4 | 3643 | 189 | 62 | S25 | -580 | 923 |
| 3 | EXTCLK | -2632 | -881 | 33 | C5 | 3643 | 314 | 63 | S26 | -705 | 923 |
| 4 | EXT_INT | -2232 | -881 | 34 | C6 | 3643 | 439 | 64 | S27 | -830 | 923 |
| 5 | VSS | -1832 | -881 | 35 | C7 | 3643 | 564 | 65 | S28 | -955 | 923 |
| 6 | VSS | -1707 | -881 | 36 | C8 | 3643 | 689 | 66 | S29 | -1080 | 923 |
| 7 | VSS | -1582 | -881 | 37 | DUMMY | 3643 | 923 | 67 | S30 | -1205 | 923 |
| 8 | VDD | -1182 | -881 | 38 | S1 | 2464 | 923 | 68 | S31 | -1330 | 923 |
| 9 | VDD | -1057 | -881 | 39 | S2 | 2329 | 923 | 69 | S32 | -1455 | 923 |
| 10 | VDD | -932 | -881 | 40 | S3 | 2204 | 923 | 70 | S33 | -1580 | 923 |
| 11 | V5 | -532 | -881 | 41 | S4 | 2079 | 923 | 71 | S34 | -1705 | 923 |
| 12 | V5 | -407 | -881 | 42 | S5 | 1954 | 923 | 72 | S35 | -1830 | 923 |
| 13 | V5 | -282 | -881 | 43 | S6 | 1829 | 923 | 73 | S36 | -1955 | 923 |
| 14 | V5 | 117 | -881 | 44 | S7 | 1704 | 923 | 74 | S37 | -2080 | 923 |
| 15 | V2 | 517 | -881 | 45 | S8 | 1579 | 923 | 75 | S38 | -2205 | 923 |
| 16 | RESETB | 917 | -881 | 46 | S9 | 1454 | 923 | 76 | S39 | -2330 | 923 |
| 17 | RS | 1317 | -881 | 47 | S10 | 1329 | 923 | 77 | S40 | -2463 | 923 |
| 18 | R/W | 1717 | -881 | 48 | S11 | 1204 | 923 | 78 | DUMMY | -3642 | 923 |
| 19 | E | 2117 | -881 | 49 | S12 | 1079 | 923 | 79 | C16 | -3643 | 689 |
| 20 | DB0 | 2521 | -881 | 50 | S13 | 954 | 923 | 80 | C15 | -3643 | 564 |
| 21 | DB1 | 2697 | -881 | 51 | S14 | 829 | 923 | 81 | S14 | -3643 | 439 |
| 22 | DB2 | 2871 | -881 | 52 | S15 | 704 | 923 | 82 | S13 | -3643 | 314 |
| 23 | DB3 | 3047 | -881 | 53 | S16 | 579 | 923 | 83 | S12 | -3643 | 189 |
| 24 | DUMMY | 3643 | -881 | 54 | S17 | 454 | 923 | 84 | S11 | -3643 | 64 |
| 25 | DB4 | 3643 | -717 | 55 | S18 | 329 | 923 | 85 | S10 | -3643 | -60 |
| 26 | DB5 | 3643 | -591 | 56 | S19 | 204 | 923 | 86 | C9 | -3643 | -184 |
| 27 | DB6 | 3643 | -467 | 57 | S20 | 71 | 923 | 87 | TEST | -3643 | -341 |
| 28 | DB7 | 3643 | -341 | 58 | S21 | -70 | 923 | 88 | DUMMY | -3643 | -467 |
| 29 | C1 | 3643 | -184 | 59 | S22 | -205 | 923 | 89 | DUMMY | -3643 | -592 |
| 30 | C2 | 3643 | -60 | 60 | S23 | -330 | 923 | 90 | DUMMY | -3643 | -717 |

## PIN DESCRIPTION

| Pin | Input/Output | Name | Description | Interface |
|---|---|---|---|---|
| VDD | P | Power supply & LCD Bias pin | for logical circuit (+3v, +5v) | Power Supply |
| VSS(GND) | | | 0V (GND) | |
| V2, V3, V5 | | | Bias voltage level for LCD driving | |
| S1 ~ S40 | Output | Segment output | Segment signal output for LCD driving | LCD |
| C1 ~ C16 | Output | Common output | Common signal output for LCD driving | LCD |
| EXTCLK | Input | External clock Input | When using external clock, used as clock input pin. When using internal oscillator, connect to VDD or VSS. | External clock |
| EXT_INT | Input | External/Internal oscillator clock select | When EXT_INT = “High”, external clock is used. When “Low”, internal oscillator is used. | MPU |
| RS | Input | Register select | Used as register selection input. When RS= “High”, Data register is selected. When RS= “Low”, Instruction register is selected. | MPU |
| R/W | Input | Read/Write | Used as read/write selection input. When RW=“High”,read operation. When RW=“Low”, write operation. | |
| E | Input | Read/Write enable | Used as read/write enable signal. | |
| DB0 ~ DB3 | Input/Output | Data Bus 0 ~ 7 | When 8-bit bus mode, used as low order bidirectional data bus. During 4-bit bus mode open these pins. | |
| DB4 ~ DB7 | | | When 8-bit bus mode, used as high order bidirectional data bus. IN case of 4-bit bus mode, used as both high and low order. DB7 is used for Busy Flag output during read instruction operation. | |
| RESETB | Input | Reset | If it is necessary to initialize the system by hardware, force “Low”, level signal to this terminal about 1.2 mS. | |
| TEST | Output | Test Pin | Internal oscillator test pin. Openthis pin. | |

## FUNCTION DESCRIPTION

System Interface

This chip consists of two kinds of interface type with MPU : 4-bit bus and 8-bit bus.
4-bit bus and 8-bit bus is selected by DL bit of function set in the instruction register.

During read or write operation, two 8-bit registers are used. One is the data register (DR), the other is the instruction register (IR).

The data register (DR) is used as a temporary data storage place for being written into or read from DDRAM/CGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically.
Thus, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register (IR) is used only to store instruction code transferred from MPU.
MPU cannot read data from instruction register.

The register selection depends on RS input pin setting in both 4-bit bus mode.

**Table 1. Various kinds of operations according to RS and R/W bits.**

| RS | R/W | Operation |
|---|---|---|
| 0 | 0 | Instruction Write operation (MPU writes Instruction code into IR) |
| 0 | 1 | Read Busy flag (DB7) and address counter (DB0 ~ DB6) |
| 1 | 0 | Data Write operation (MPU writes data into DR) |
| 1 | 1 | Data Read operation (MPU reads data from DR) |

Busy Flag (BF)

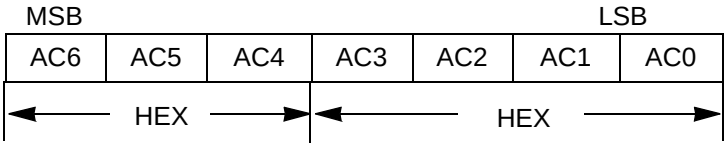
BF = “High” it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read instruction Operation), through DB7 port.
Before excuting the next instruction, be sure that BF is not High.

Address Counter (AC)

Address Counter (AC)stores the address of DDRAM/CGRAM that are transferred from IR.
After writing into (reading from) DDRAM/CGRAM data, AC is increased (decreased) by 1 automatically.
When RS = “Low”, and R/W = “High”, AC value can be read through DB0 ~ DB6 ports.

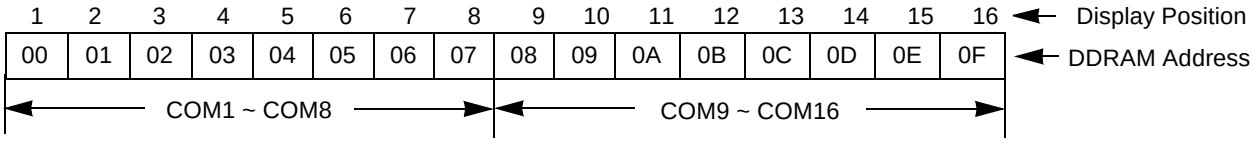
Display Data RAM (DDRAM)

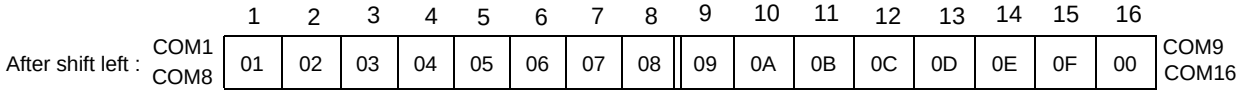
DDRAM stores 8bits character code in CGROM/CGRAM and its maximum number is 16 (16 Characters).
DDRAM address is set by the address counter (AC) as a hexadecimal number.

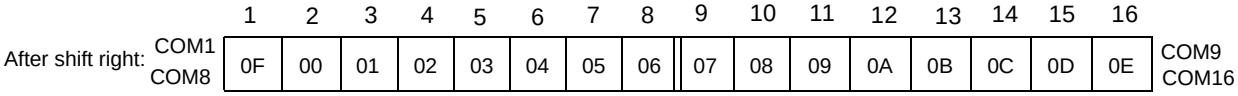



The relations of DDRAM address and display position is as follows.

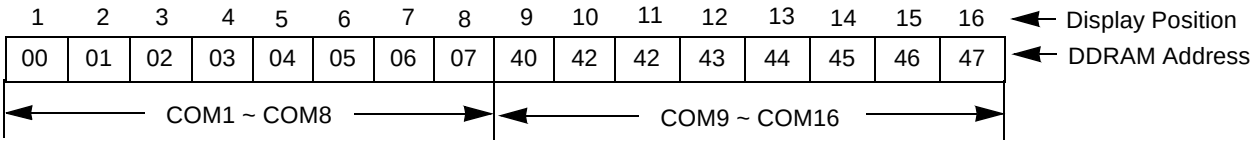
1) DDRAM addressing mode 0 (A=0)
In this addressing mode, the address range of DDRAM is 00H ~ 0FH.

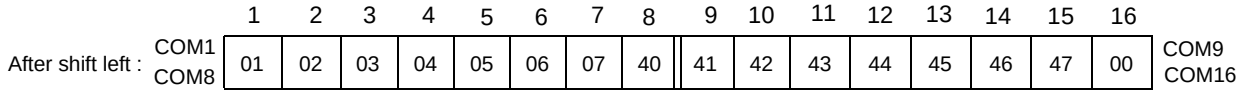


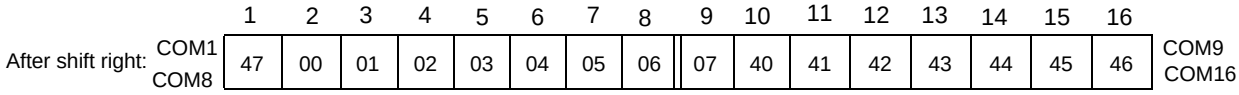




2) DDRAM addressing mode 1 (A=1)
In this addressing mode, the address range of DDRAM is 00H ~ 07H and 40H ~ 47H.



Character Generator RAM (CGRAM)

CGRAM is used for user defined character pattern. The format of the character pattern is 5 X 7 dots except for the cursor position and has a maximum of 4 characters. To use the character pattern in CGRAM write the character code intoDDRAM as shown in table 2.

**Table 2. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)**

| Character Code(DDRAM data) | | | | | | | | CGRAM address | | | | | CGRAM data | | | | | Pattern Number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 4 | 3 | 2 | 1 | 0 | 4 | 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 | * | * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | |
| | | | | | | | | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Pattern 1 |
| | | | | | | | | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | <-- cursor position |
| | | | | . | | | | | . | | . | | | | . | | | . |
| | | | | . | | | | | . | | . | | | | . | | | . |
| | | | | . | | | | | . | | . | | | | . | | | . |
| | | | | . | | | | | . | | . | | | | . | | | . |
| 0 | 0 | 0 | 0 | * | * | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | |
| | | | | | | | | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | Pattern 4 |
| | | | | | | | | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | |
| | | | | | | | | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | <-- Cursor position |

**NOTE** : the asterisk means “don’ t care”.

Character Generator ROM (CGROM)

CGROM generates 5 X 8 character pattern from character generate code in DDRAM. CGROM has 5 X 8-dot 240 character pattern including cursor position. If the data in cursor position bit are high, the data are included to the character pattern. So, the slected positions are always ON regardless to cursor position.
The relationship between character code and character pattern can be referred to table 3.

Timing Generation Circuit

Timing generation circuit generates clock signals for the internal operations.

LCD Driver Circuit

LCD driver circuit has 16 common and 40 segment output signals for LCD driving.
Data from CGRAM/CGROM is transferred to 40-bit segment shift register in a serially, which is then it is stored to 40-bit segment output latch. When each com is selected by a 16-bit common register, the segment data also outputs through segment driver from 40-bit segment output latch.

Cursor/Blink Control Circuit

It controls cursor/blink ON/OFF at the cursor position.

## INSTRUCTION DESCRIPTION

OUTLINE

To overcome the speed difference between the internal clock of KS0072 and the MPU clock, the KS0072 performs an internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bys.
Instruction can be divided into four types:

(1) KS0072 function set instructions (set display methods, set data length, etc.)
(2) Address set instructions to internal RAM
(3) Data transfer instructions with internal RAM
(4) Others
The address of internal RAM is automatically increased or decreased by 1.

* Note : During an internal operation, the Busy Flag (DB7) is High. Busy Flag check must precede the next instruction.

**Table 3. Instruction Table**

| Instruction | | Instruction Code | | | | | | | | | | Description | Execution time (fosc=270 kHZ) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | RS | R/W | DB 7 | DB 6 | DB 5 | DB 4 | DB 3 | DB 2 | DB 1 | DB 0 | | |
| Test Mode | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Device test mode (When 4-bit interface mode) No operation (When 8-bit interface mode) | - |
| Clear Display | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write “20H” to DDRAM and set DDRAM address to “20H” from AC. | 629µs |
| Return Home | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | Set DDRAM address to “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed. | 629µs |
| Entry Mode Set | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1/D | S | Assign cursor moving direction and enable entire dispaly shift. | 37µs |
| Display ON/ OFF Control | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | All display(D), cursor(C), and blinking of cursor position character on/off control bit(B). | 37µs |
| Cursor or Display Shift | | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | * | * | Cursor and Display shift and their direction control without changing DDRAM data. | 37µs |
| Function Set | | 0 | 0 | 0 | 0 | 1 | DL | A | * | M1 | M0 | Set interface data length(DL), DDRAM addressing mode (A) and COM/SEG output pattern(M0,M1). | 37µs |
| Set CGRAM Address | | 0 | 0 | 0 | 1 | * | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in address counter. | 37µs |
| Set DDRAM Address | | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address in address counter. | 37µs |
| Read Busty flag and Address | DDRAM | 0 | 1 | BF | AC6 | AC6 | AC4 | AC3 | AC2 | AC1 | AC0 | Whether in internal operation or not can be known by reading BF. The contents of address counter can also be read. | 0µs |
| | CGRAM | | | | * | * | AC4 | AC3 | AC2 | AC1 | AC0 | | |
| Write Data to RAM | DDRAM | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write data into internal RAM (DDRAM/CGRAM). | 43µs |
| | CGRAM | | | * | * | * | D4 | D3 | D2 | D1 | D0 | | |
| Read Data from RAM | DDRAM | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Read data from internal RAM (DDRAM/CGRAM). | 43µs |
| | CGRAM | | | * | * | * | D4 | D3 | D2 | D1 | D0 | | |

**NOTE** : the asterisk means “don’t care”.

| | | | | | |
|---|---|---|---|---|---|
| I/D = 1 | : | Increment, | I/D = 0 | : | Decrement |
| S = 1 | : | Shift enable | S = 1 | : | Shift disable |
| S/C = 1 | : | Display shift, | S/C = 0 | : | Move cursor |
| R/L = 1 | : | Shift right, | R/L = 0 | : | Shift left |
| D/L = 1 | : | 8 bit interface, | D/L = 0 | : | 4 bit interface |
| A = 0 | : | DDRAM addressing mode 0, | A = 1 | : | DDRAM addressing mode1 |
| M0 = 0 | : | COM/SEG output pattern A, | M0 = 1 | : | COM/SEG output pattern B |
| M1 = 0 | : | 1 line 16 characters, | M1 = 1 | : | 2 line 8 characters |
| BF = 1 | : | System is in operation | BF = 0 | : | System is ready |

Contents

1) Test Mode

| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

After setting the DL bit to 4-bit data interface mode (DL=0), writing this code twice makes the system go to test mode. And when 8-bit interface mode (DL=1) is set, normal function mode is returned.
System is unaffected if this code is set in 8-bit interface, other than consuming some time. (37 μs at fosc=270KHz)

2) Clear Display

| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Clear all the display data by writing "20H" (space code of CGROM) to all DDRAM address, and set DDRAM address to "00H" into AC (Address Counter). For this instruction, the CGROM address "20H" has to be set to space code. Shifting of the display position returns it to the original position. Namely, when display data is disappeared and cursor or blinking is displayed, bring the cursor to the left edge on first line of the display. It makes entry mode to increment (I/D=1)

3) Return Home

| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * |

"*" : Don't care

Set DDRAM address to "00H" into the address counter. Shifting of the display position returns it to the original position. When cursor or blinking is displayed, bring the cursor to the left edge on first line of the display. The data in DDRAM does not change.

4) Entry Mode Set

| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S |

Set the moving direction of cursor and display.

**I/D : Increment/decrement of DDRAM/CGRAM address (cursor or blink)**

When I/D="High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D="Low", cursor/blink moves to left and DDRAM address is decresed by 1.

**S : Shift of entire display**

When DDRAM read (CGRAM read/write)operation or S= "Low", entire display is not shift.
If S="High", and DDRAM write operation, entire display is sifted according to I/D value (I/D="1" : shift left, I/D="0" : shift right).

5) Display ON/OFF Control

| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B |

Control display /cursor/blink ON/OFF 1 bit register.

**D : Display ON/OFF control bit**
When D = “High”, entire display is turned on.
When D = “Low”, entire display is turned off, but display data is remains in DDRAM.

**C : Cursor ON/OFF control bit**
When C = “High”, cursor is turned on.
When C = “Low”, cursor is disappeared in current display, but I/D register preserves its data.

**B : Cursor Blink ON/OFF control bit**
When B = “High”, cursor blink is on, performs alternately between all high data (black pattern)and display character at the cursor position.
When B =“Low”, blink is off.

6) Cursor or Display Shift

| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | * | * |

“*” : Don’t care

Without writing or reading of display data, shift right/left the cursor position or display.
This instruction is used to correct or search display data. (Refer to Table 5)
During 2-line mode display, cursor moves to the 2nd line after 8th digit of 1st line.
Note that display shift is performed simultaneously in all the line.
When displayed data is shifted repeatedly, each line is shifted individually.
When display shift is performed, the contents of address counter are not changed.

**Table 4. Shift patterns accoring to S/C and R/L bits**

| S/L | R/L | Operation |
|---|---|---|
| 0 | 0 | Shift cursor to the left, AC is decreased by 1 |
| 0 | 1 | Shift cursor to the right, AC is increased by 1 |
| 1 | 0 | Shift all the display to the left, cursor moves according to the display |
| 1 | 1 | Shift all the display to the right, cursor moves according to the display |

7) Function Set

| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 0 | 0 | 1 | DL | A | * | M1 | M0 |

"*" : Don't care

**DL : Interface data length control bit**

When DL = "High", 8-bit bus mode with MPU.
When DL = "Low", 4-bit bus mode with MPU. Thus, DL is a signal to select 8-bit or 4-bit bus mode.
In 4-bit bus mode, the 4-bit data is transsferred twice.

**A : Set the display data addressing mode**

When A = "Low", DDRAM addressing mode 0.
When A = "High", DDRAM addressing mode 1.

**MO : Set COM/SEG output rotation**

When M0 = "Low", COM/SEG output rotation mode A.
When M0 = "High", COM/SEG output rotation mode B.

**M1 : Set display line and character mode**

When M1 = "Low", 1 line 16 character display mode.
When M1 = "High", 2line 8 character display mode.
(Refer to Application information)

8) Set CGRAM Address

| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 0 | 1 | * | AC4 | AC3 | AC2 | AC1 | AC0 |
| | | | | | | MSB | | | | LSB |

"*" : Don't care

Set CGRAM address to AC.
This instruction allows the MPU to access CGRAM data for user defined character pattern.
Available CGRAM Address is lower 5 bits (DB4 ~ DB0).

9) Set DDRAM Address

| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

"*" : Don't care

Set DDRAM address to AC.
This instruction allows the MPU to access DDRAM data.
When DDRAM addressing mode 1 (A=0), DDRAM address is from "00H" to "0FH".
In DDRAM addressing mode 2 (A=1), DDRAM address range of the 1st 8 character is "00H" to "07H", and DDRAM address range of the 2nd 8 character is "40H" to "47H".

10) Read Busy Flag & Address

| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | DDRAM |
| | | | | MSB | | | | | | LSB | |

| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | BF | * | * | AC4 | AC3 | AC2 | AC1 | AC0 | CGRAM |
| | | | | | | MSB | | | | LSB | |

This instruction shows whether KS0072 is in internal operation or not. If the resultant BF is High, The internal operation is in progress and should wait until BF to be Low, which by then the next instruction can be performed.
In the instruction you can read also the value of address counter.

11) Write data to RAM

| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (DDRAM) |
| | | | MSB | | | | | | | LSB | |

| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | * | * | * | D4 | D3 | D2 | D1 | D0 | (CGRAM) |
| | | | | | | MSB | | | | LSB | |

"*" : Don't care

Write binary 8/5 bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM/CGRAM is set by the previous address set instruction (DDRAM address set, CGRAM address set).
After writing operation, the address is automatically increased/decreased by 1, according to the entry mode.

12) Read data from RAM

| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (DDRAM) |
| | | | MSB | | | | | | | LSB | |

| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | * | * | * | D4 | D3 | D2 | D1 | D0 | (CGRAM) |
| | | | | | | MSB | | | | LSB | |

"*" : Don't care

Read bINARY 8/5 bit from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, data that was read first becomes invalid, as the direction of AC is not determined. If RAM data is read several times without RAM address set instruction before read operation, the correct RAM data can be detained from the second, but the first data would be incorrect, as there is no time margin to transfer the RAM data. In case of DDRAM reading operation, the cursor shift instruction plays the same role as DDRAM address set instruction also transfers RAM data to output data register.
After read operation address counter is automatically increased/decreased by 1 according to the entry mode.
After CGRAM read operation is , the display shift may not be executed correctly.

* In case of RAM write operation, AC is increasd/decreased by 1 like read operation (after this operation).
  In this time, AC indicates the next address position, but only the previous data can be read by read instruction.

## INTERFACE WITH MPU

Interface with 8-bit MPU

With 8-bit interfacing data length transfer is performed at a time through 8 ports, from DB0 to DB7.
Example of timing sequence is shown below.

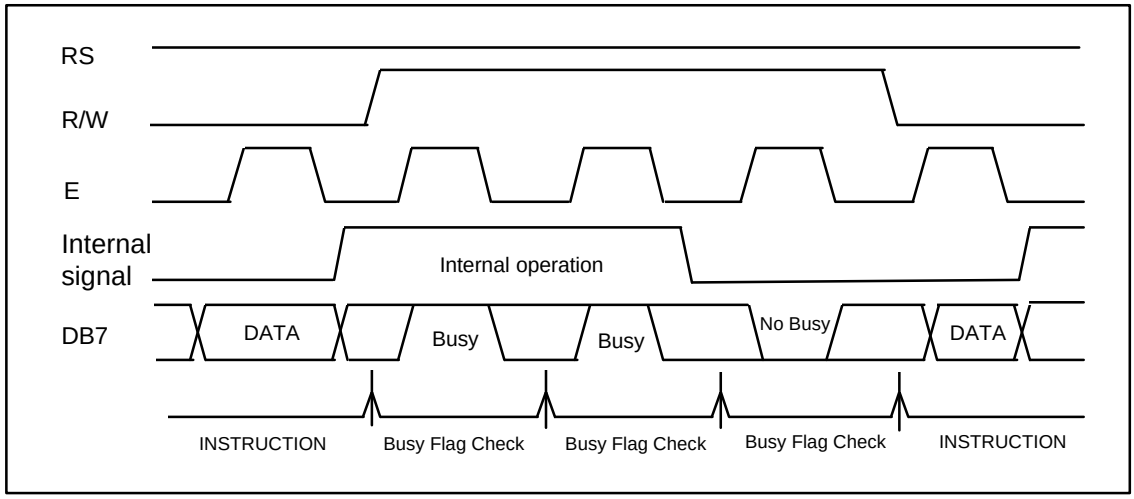



**Fig 1. Example of 8-bit Bus Mode Timing Diagram**

Interface with 4-bit MPU

When interfacing data length are 4-bit, only 5 ports, from DB4 to DB7, are used as data bus.
Af first higher 4-bit (in case of 8-bit bus mode, the contents of DB4-DB7) are transferred, then the lower 4-bit (in case of 8-bit bus mode, the contents of DB0-DB3) are transferred. So transfer is performed twice.
Busy Flag outputs “High” after the second transfer are ended.
Example of timing sequence is shown below.

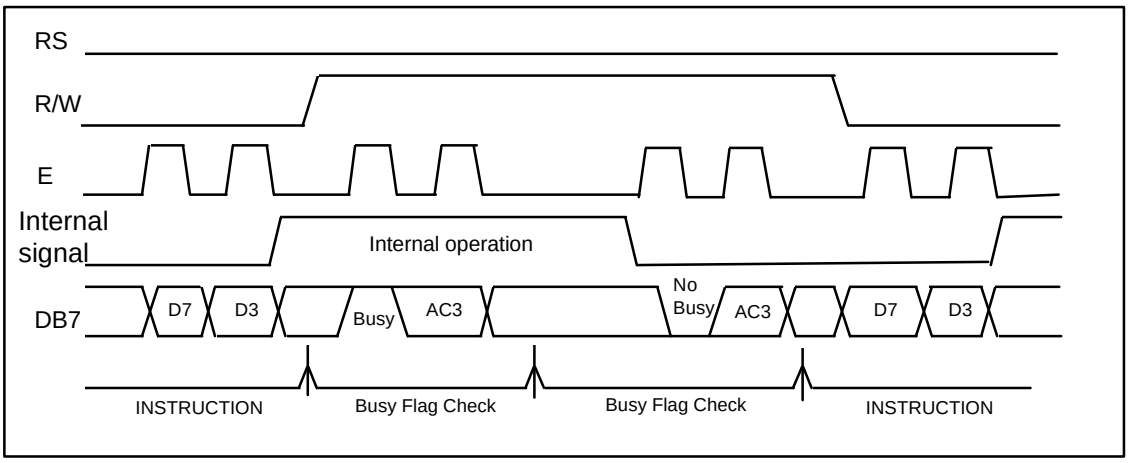
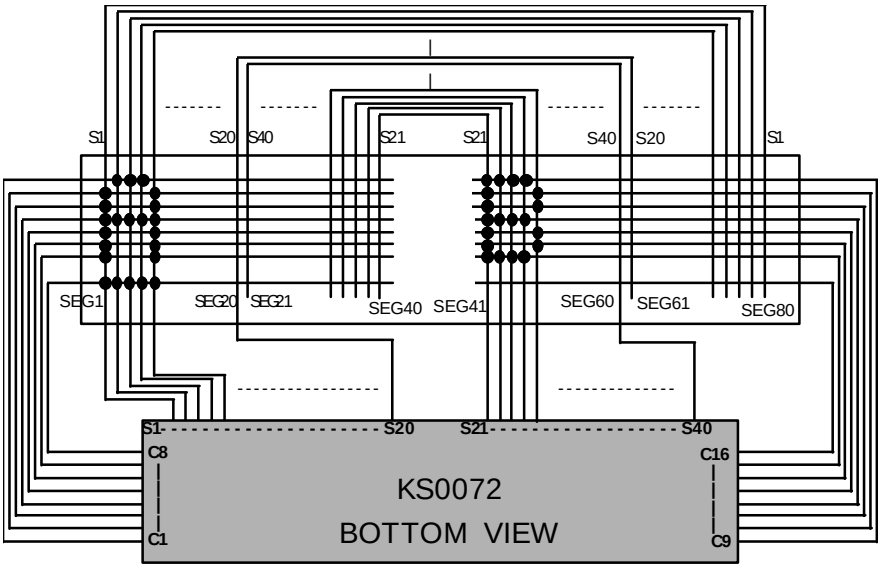



**Fig 2. Example of 4-bit Bus Mode Timing Diagram**

## APPLICATION INFORMATION

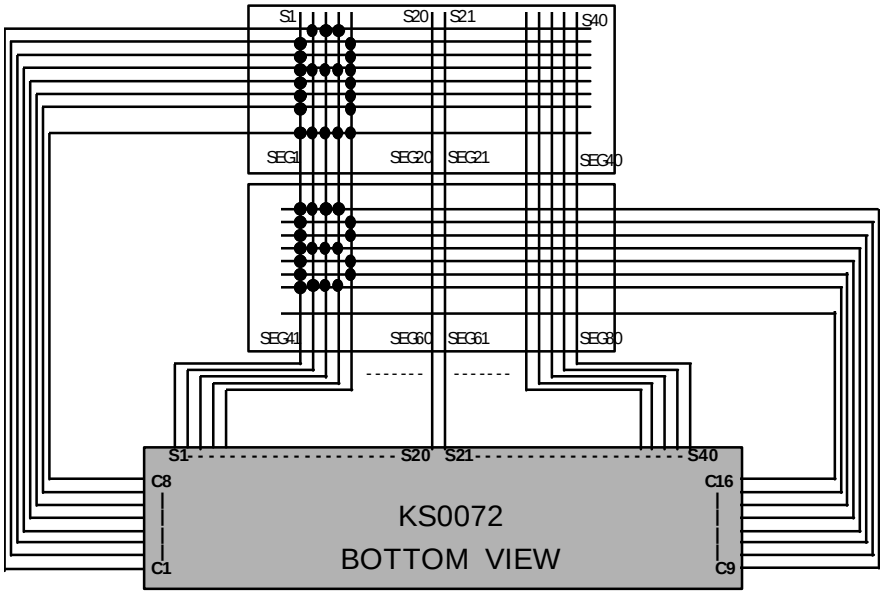
COM/SEG output rotation mode A

1) DDRAM address mode 0 (A=0)




( M0=0, M1=0 )

2) DDRAM address mode 1 (A=1)

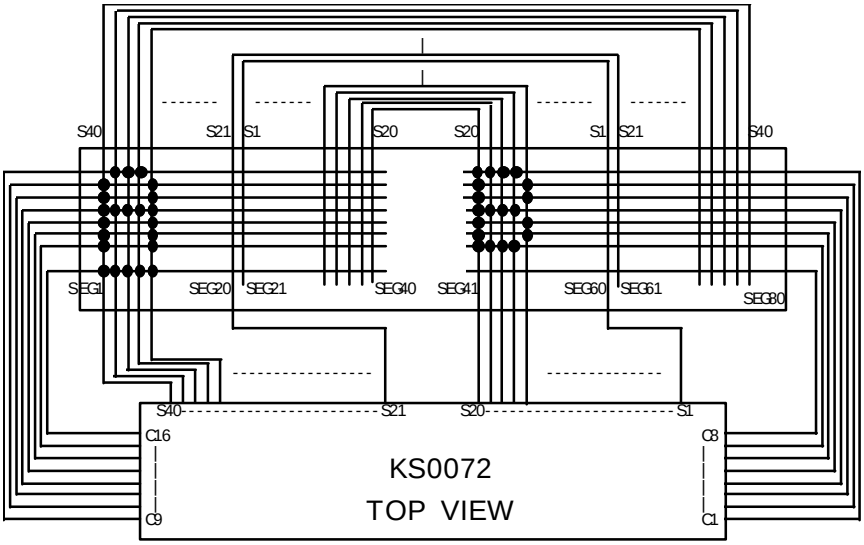



( M0=0, M1=1 )

## APPLICATION INFORMATION

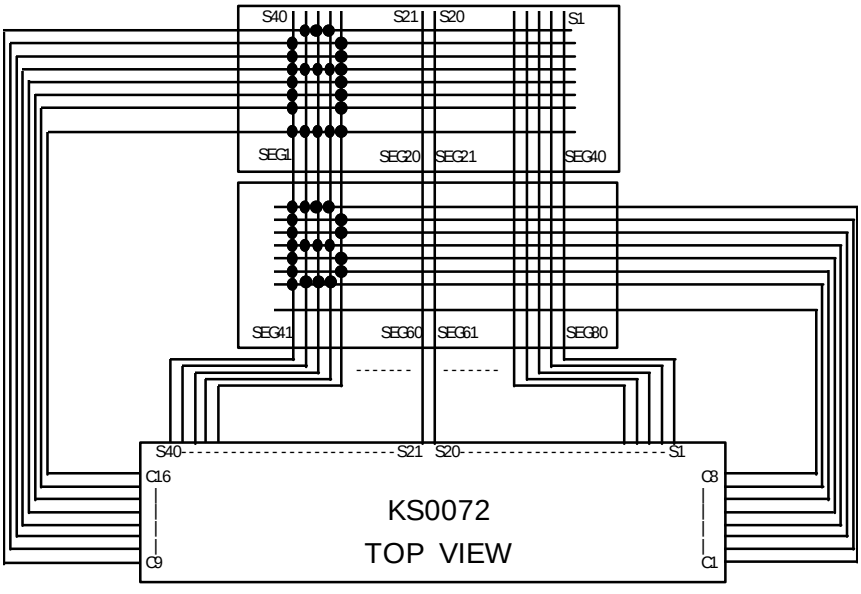
COM/SEG output rotation mode B

1) DDRAM address mode 0 (A=0)



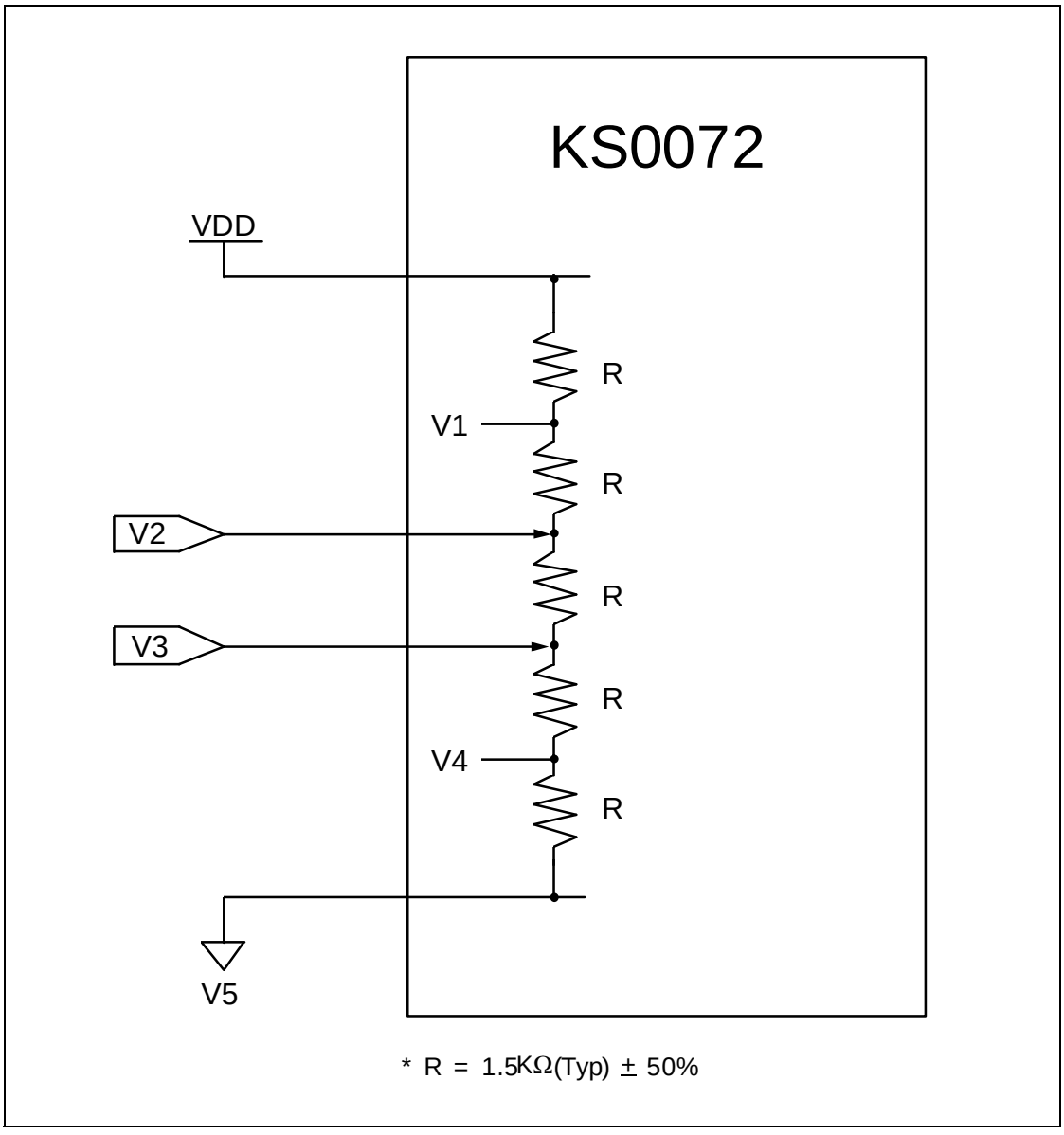

( M0=1, M1=0 )

2) DDRAM address mode 1 (A=1)




( M0=1, M1=1 )

**POWER SUPPLY FOR DRIVING LCD PANEL**



## INTIALIZING

### Initialize by internal power-on-reset circuit

When the power is turned on, KS0072 is initialized automatically by power on reset circuit.
During the initialization, the following instructions are executed, and BF (Busy Flag) is kept "High" (busy state) up to the end of initialization.

**Initialize flow**

**1) Display Clear**

Write "20H" to all DDRAM

**2) Set Functions**

DL = 1 : 8-bit bus mode
A = 0 : DDRAM addressing mode 1
M0 = 0 : COM/SEG output rotation mode A
M1 = 0 : 1 line 16 character display mode

**3) Control Display ON/OFF instruction**

D = 0 : Display OFF
C = 0 : Cursor OFF
B = 0 : Blink OFF

4) Set Enty Mode

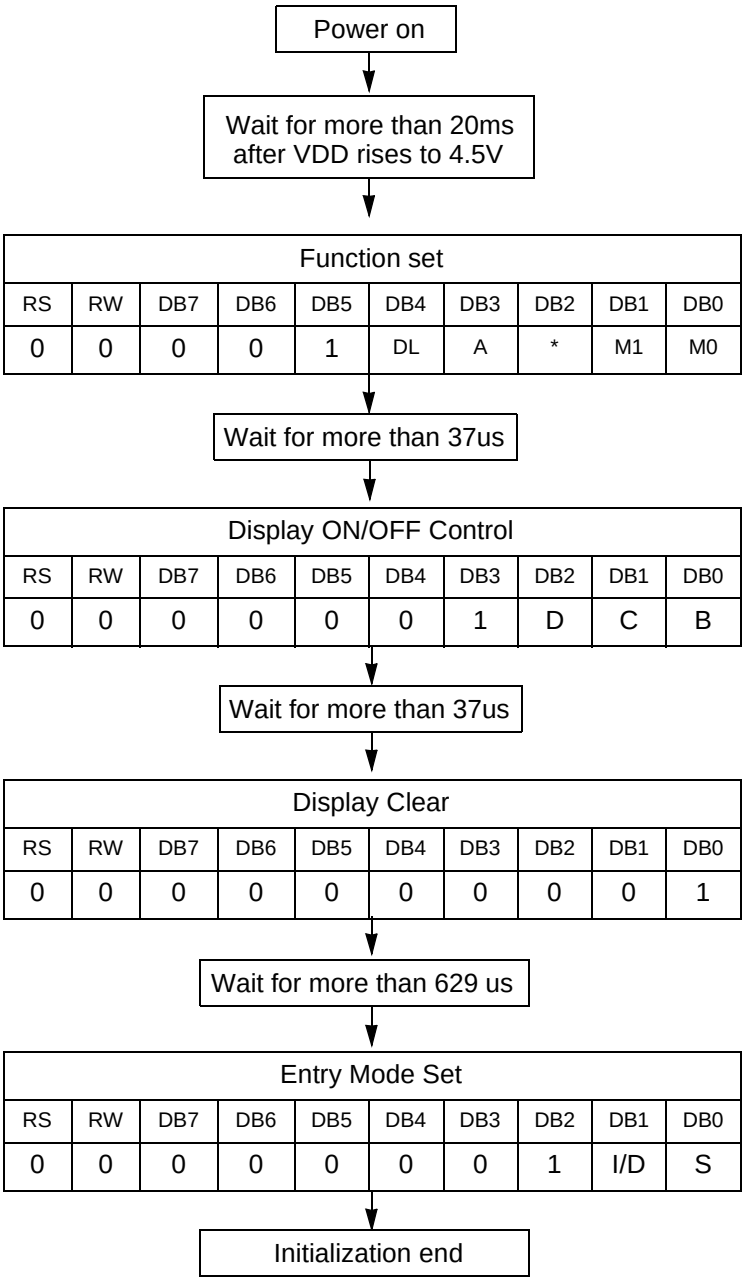
I/D = 1 : Increment by 1
S = 0 : No entire display shift

Initialize by external hardware reset

If the £¢Low£¢ signal is forced to reset terminal over a period of 1.2 ms then system will be initialized.
And BF (Busy Flag) is kept "High" (busy state) for 629 us after releasing the initializing sequence.

Initializing by instruction

1) 8-bit interface mode



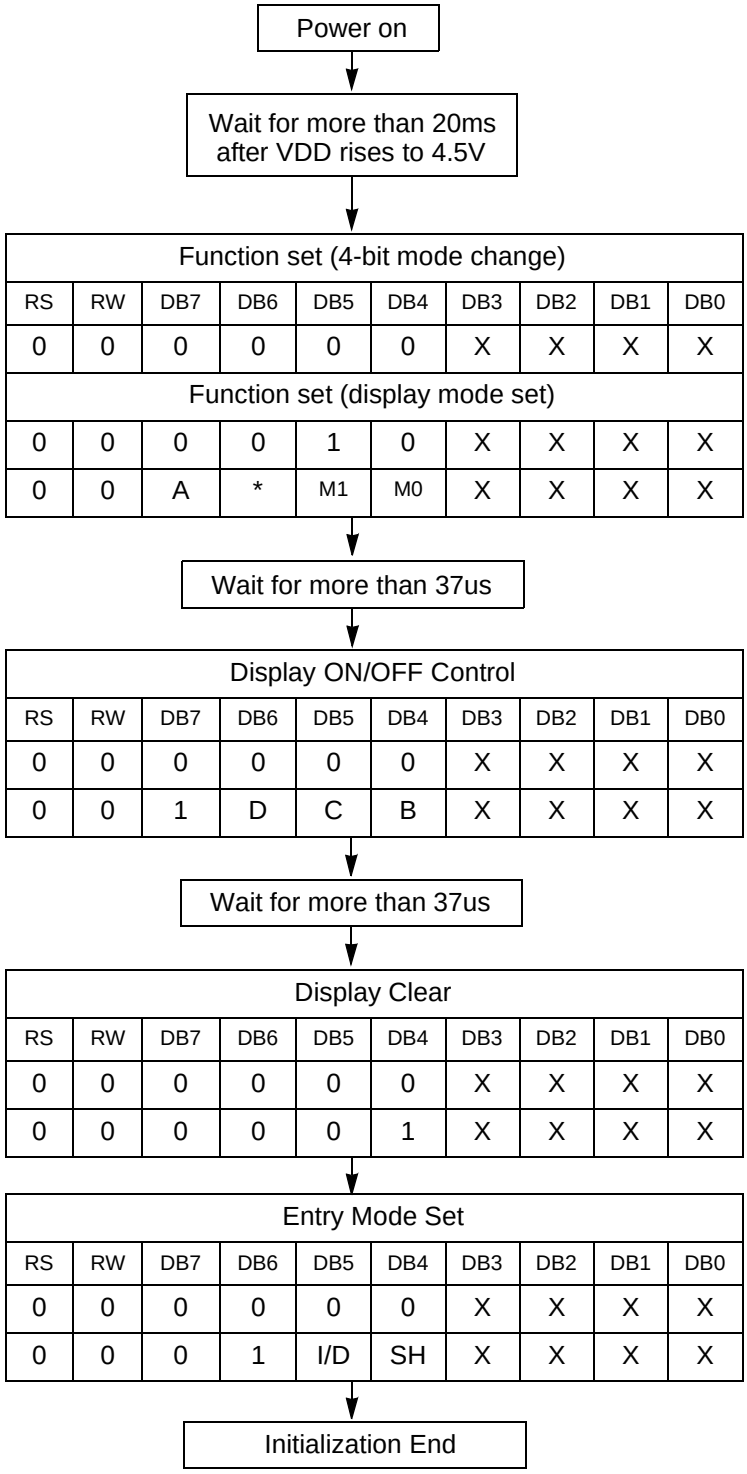

Condition : $f_{OSC}$ = 270KHz

| | | |
|---|---|---|
| DL | 0 | 4-bit interface |
| | 1 | 8-bit interface |
| A | 0 | DDRAM Addressing mode1 |
| | 1 | DDRAM Addressing mode2 |
| M0 | 0 | COM/SEG output rotation mode A |
| | 1 | COM/SEG output rotation mode B |
| M1 | 0 | 1line 16 character display mode |
| | 1 | 2line 8 character display mode |

| | | |
|---|---|---|
| D | 0 | display off |
| | 1 | display on |
| C | 0 | cursor off |
| | 1 | cursor on |
| B | 0 | blink off |
| | 1 | blink on |

| | | |
|---|---|---|
| I/D | 0 | decrement mode |
| | 1 | increment mode |
| S | 0 | entire shift off |
| | 1 | entire shift on |

2) 4-bit interface mode




| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | X |
| 0 | 0 | 0 | 0 | 1 | 0 | X | X | X | X |
| 0 | 0 | A | * | M1 | M0 | X | X | X | X |

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | X |
| 0 | 0 | 1 | D | C | B | X | X | X | X |

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | X |
| 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | X |

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | X |
| 0 | 0 | 0 | 1 | I/D | SH | X | X | X | X |

Condition : $f_{OSC}$ = 270KHz

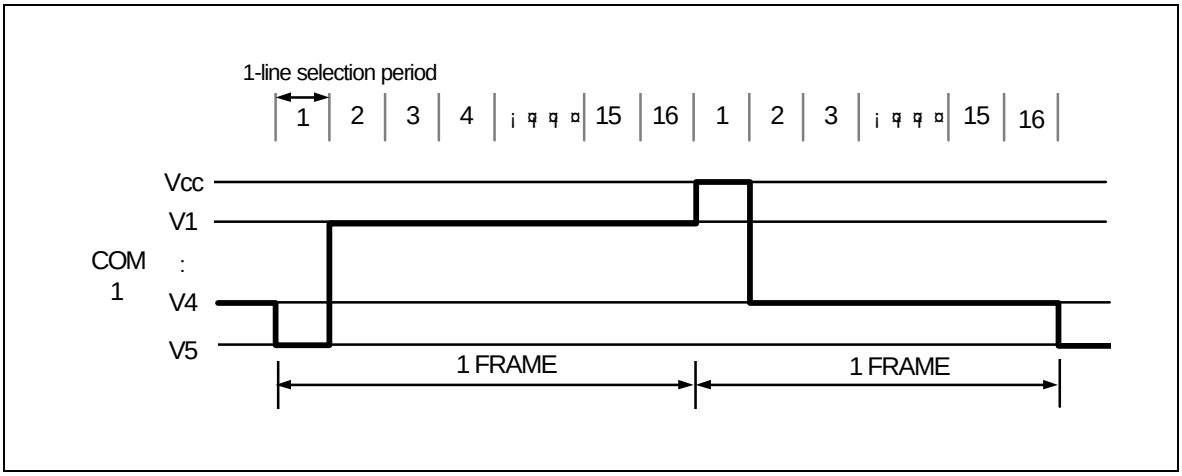
| | | |
|---|---|---|
| DL | 0 | 4-bit interface |
| | 1 | 8-bit interface |
| A | 0 | DDRAM Addressing mode1 |
| | 1 | DDRAM Addressing mode2 |
| M0 | 0 | COM/SEG output rotation mode A |
| | 1 | COM/SEG output rotation mode B |
| M1 | 0 | 1line 16 character display mode |
| | 1 | 2line 8 character display mode |

| | | |
|---|---|---|
| D | 0 | display off |
| | 1 | display on |
| C | 0 | cursor off |
| | 1 | cursor on |
| B | 0 | blink off |
| | 1 | blink on |

| | | |
|---|---|---|
| I/D | 0 | decrement mode |
| | 1 | increment mode |
| S | 0 | entire shift off |
| | 1 | entire shift on |

## FRAME FREQUENCY

1/16 duty cycle




1-Line selection period = 160 clocks
One Frame = 40 x 16 x 3.7µs x 4 = 9.472ms (1 CLOCK = 3.7µs at fosc=270KHz)
Frame frequency = 1 / 9.472ms = 105.6Hz

## MAXIMUM ABSOLUTE LIMIT

Maximum absolute Power Ratings

| Item | Symbol | Unit | Value |
|---|---|---|---|
| Power supply voltage (1) | $V_{DD}$ | V | -0.3 to + 7.0 |
| Power supply voltage (2) | $V_{LCD}$ | V | -0.3V TO + 13V |
| Input voltage | $V_{IN}$ | V | -0.3 to VDD + 0.3 |

* Voltage greater than above may damage to the circuit (VDD $\geq$ V2 $\geq$ V3 $\geq$ V5, VLCD = VDD-V5)

Temperature Characteristics

| Item | Symbol | Unit | Value |
|---|---|---|---|
| Operating temperature | Topr | $^{o}C$ | -30 to + 85 |
| Storage temperature | Tstg | $^{o}C$ | -55 to +125 |

## ELECTRICAL CHARACTERISTICS

DC Characteristics

($V_{DD}$ = 4.5V to 5.5V, Ta = -30 to + 85 °C)

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | $V_{DD}$ | - | 4.5 | - | 5.5 | V |
| Supply Current | $I_{DD}$ | Internal oscillation ($V_{DD}$ = 5.0V, fosc=270KHz) | - | 1.0 | 1.8 | mA |
| Input Voltage (1) (except OSC1) | $V_{IH1}$ | - | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| | $V_{IL1}$ | - | -0.3 | - | 0.8 | |
| Input Voltage (2) (OSC1) | $V_{IH2}$ | - | $V_{DD}$-1.0 | - | $V_{DD}$ | V |
| | $V_{IL2}$ | - | -0.2 | - | 1.0 | |
| Input Voltage (2) (E pin) | $V_{IH3}$ | - | $0.8V_{DD}$ | - | $V_{DD}$ | V |
| | $V_{IL3}$ | - | - | - | $0.2V_{DD}$ | |
| Output Voltage (1) (DB0 to DB7) | $V_{OH1}$ | $I_{OH}$ = -0.205 (mA) | 2.4 | - | - | V |
| | $V_{OL1}$ | $I_{OL}$ = 1.6 (mA) | - | - | 0.4 | |
| Output Voltage (2) (except DB0-to DB7) | $V_{OH2}$ | $I_O$=-40 (μA) | $0.9V_{DD}$ | - | - | V |
| | $V_{OL2}$ | $I_O$=40 (μA) | - | - | $0.1V_{DD}$ | |
| Voltage Drop | $Vd_{COM}$ | $I_O$ = ± 0.1 (mA) | - | - | 1 | V |
| | $Vd_{SEG}$ | | - | - | 1 | |
| Input Leakage Current | $I_{IL}$ | $V_{IN}$ = 0V to $V_{DD}$ | -1 | - | 1 | μA |
| Low Input Current | $I_{IN}$ | $V_{IN}$ = 0V, $V_{DD}$ = 5V (PULL UP) | -50 | -125 | -250 | |
| LCD Driving Voltage | V2 | $V_{DD}$ = 5V, V5 = 0V SEG output port | 2.7 | 3.0 | 3.3 | V |
| | V3 | | 1.7 | 2.0 | 2.3 | |
| Divide Resistor | $R_B$ | $V_{DD}$-V5=5V RB=($V_{DD}$-V5) / $I_B$ $I_B$ = Divide Resistor Current | 3.7 | 7.5 | 11.5 | kΩ |
| Interanl Clock (internal Rf) | $f_{IC}$ | $V_{DD}$ = 5V | 190 | 270 | 350 | KHz |
| LCD Driving Voltage | $V_{LCD}$ | $V_{DD}$ - 5V | 3.0 | - | 11.0 | V |

($V_{DD}$ = 2.7V to 4.5V, Ta = -30 to + 85 °C)

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | $V_{DD}$ | - | 2.7 | - | 4.5 | V |
| Supply Current | $I_{DD}$ | Internal oscillation ($V_{DD}$ = 3.0V, fosc=270KHz) | - | 0.5 | 1.2 | mA |
| Input Voltage (1) (except OSC1) | $V_{IH1}$ | - | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| | $V_{IL1}$ | - | -0.3 | - | 0.4 | |
| Input Voltage (2) (OSC1) | $V_{IH2}$ | - | $V_{DD}$-1.0 | - | $V_{DD}$ | V |
| | $V_{IL2}$ | - | -0.2 | - | $0.2V_{DD}$ | |
| Input Voltage (2) (E pin) | $V_{IH3}$ | - | $0.8V_{DD}$ | - | $V_{DD}$ | V |
| | $V_{IL3}$ | - | - | - | 0.4 | |
| Output Voltage (1) (DB0 to DB7) | $V_{OH1}$ | $I_{OH}$ = -0.1 (mA) | $0.75V_{DD}$ | - | - | V |
| | $V_{OL1}$ | $I_{OL}$ = 0.1 (mA) | - | - | $0.2V_{DD}$ | |
| Output Voltage (2) (except DB0-to DB7) | $V_{OH2}$ | $I_O$=-40 (μA) | $0.8V_{DD}$ | - | - | V |
| | $V_{OL2}$ | $I_O$=40 (μA) | - | - | $0.2V_{DD}$ | |
| Voltage Drop | $Vd_{COM}$ | $I_O$ = ± 0.1 (mA) $V_{LCD}$ = 5V | - | - | 1 | V |
| | $Vd_{SEG}$ | | - | - | 1 | |
| Input Leakage Current | $I_{IL}$ | $V_{IN}$ = 0V to $V_{DD}$ | -1 | - | 1 | μA |
| Low Input Current | $I_{IN}$ | $V_{IN}$ = 0V, $V_{DD}$ = 3V (PULL UP) | -10 | -50 | -120 | |
| LCD Driving Voltage | V2 | $V_{DD}$ = 3V, V5 = -2V SEG output port | 0.7 | 1.0 | 1.3 | V |
| | V3 | | -1.7 | 0 | 0.3 | |
| Divide Resistor | $R_B$ | $V_{DD}$-V5=5V RB=($V_{DD}$-V5) / $I_B$ $I_B$ = Divide Resistor Current | 3.7 | 7.5 | 11.5 | kΩ |
| Interanl Clock (internal Rf) | $f_{IC}$ | $V_{DD}$ = 3V | 190 | 270 | 350 | KHz |
| LCD Driving Voltage | $V_{LCD}$ | $V_{DD}$ - V5 | 3.0 | - | 11.0 | V |

### AC Characteristics

($V_{DD}$ = 4.5V to 5.5V, Ta = -30 to + 85 °C)

| Mode | Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Write Mode (Refer to Fig-3) | E Cycle Time | tc | 500 | - | - | ns |
| | E Rise / Fall Time | tr, tf | - | - | 20 | |
| | E Pulse Width (High, Low) | tw | 230 | - | - | |
| | R/W and RS Setup Time | tsu1 | 40 | - | - | |
| | R/W and RS Hold Time | th1 | 10 | - | - | |
| | Data Setup Time | tsu2 | 80 | - | - | |
| | Data Hold Time | th2 | 10 | - | - | |
| Read Mode (Refer to Fig-4) | E Cycle Time | tc | 500 | - | - | ns |
| | E Rise / Fall Time | tr, tf | - | - | 20 | |
| | E Pulse Width (High, Low) | tw | 230 | - | - | |
| | R/W and RS Setup Time | tsu | 40 | - | - | |
| | R/W and RS Hold Time | th | 10 | - | - | |
| | Data Output Delay Time | $t_D$ | - | - | 120 | |
| | Data Hold Time | $t_{DH}$ | 20 | - | - | |

($V_{DD}$ = 2.7V to 4.5V, Ta = -30 to + 85 °C)

| Mode | Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Write Mode (Refer to Fig-3) | E Cycle Time | tc | 1000 | - | - | ns |
| | E Rise / Fall Time | tr, tf | - | - | 25 | |
| | E Pulse Width (High, Low) | tw | 450 | - | - | |
| | R/W and RS Setup Time | tsu1 | 60 | - | - | |
| | R/W and RS Hold Time | th1 | 20 | - | - | |
| | Data Setup Time | tsu2 | 195 | - | - | |
| | Data Hold Time | th2 | 10 | - | - | |
| Read Mode (Refer to Fig-4) | E Cycle Time | tc | 1000 | - | - | ns |
| | E Rise / Fall Time | tr, tf | - | - | 25 | |
| | E Pulse Width (High, Low) | tw | 450 | - | - | |
| | R/W and RS Setup Time | tsu | 60 | - | - | |
| | R/W and RS Hold Time | th | 20 | - | - | |
| | Data Output Delay Time | $t_D$ | - | - | 360 | |
| | Data Hold Time | $t_{DH}$ | 5 | - | - | |

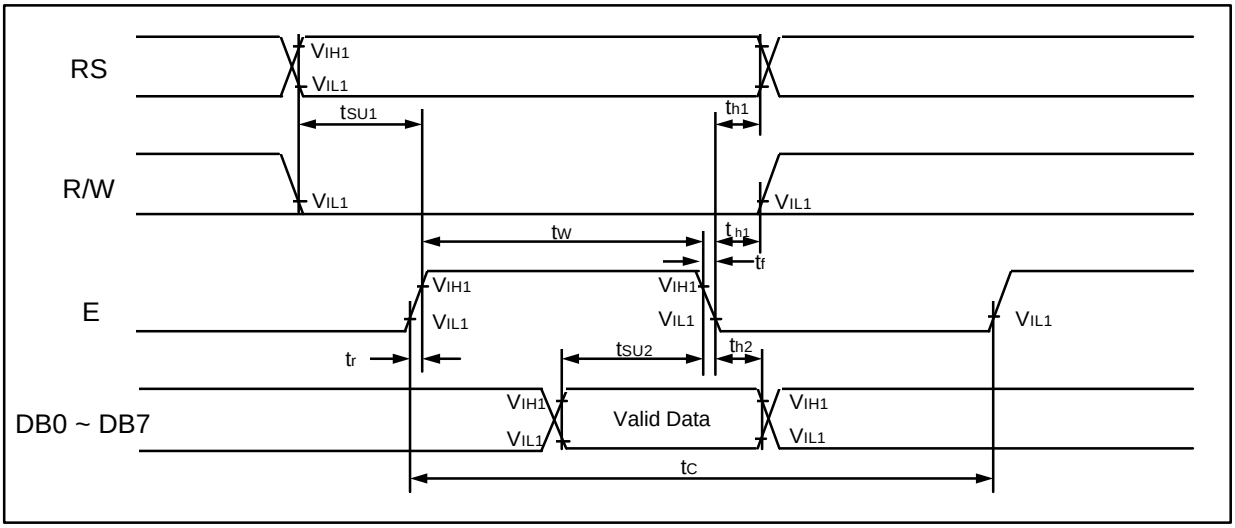



**Fig-3. Write Mode Timing Diagram**

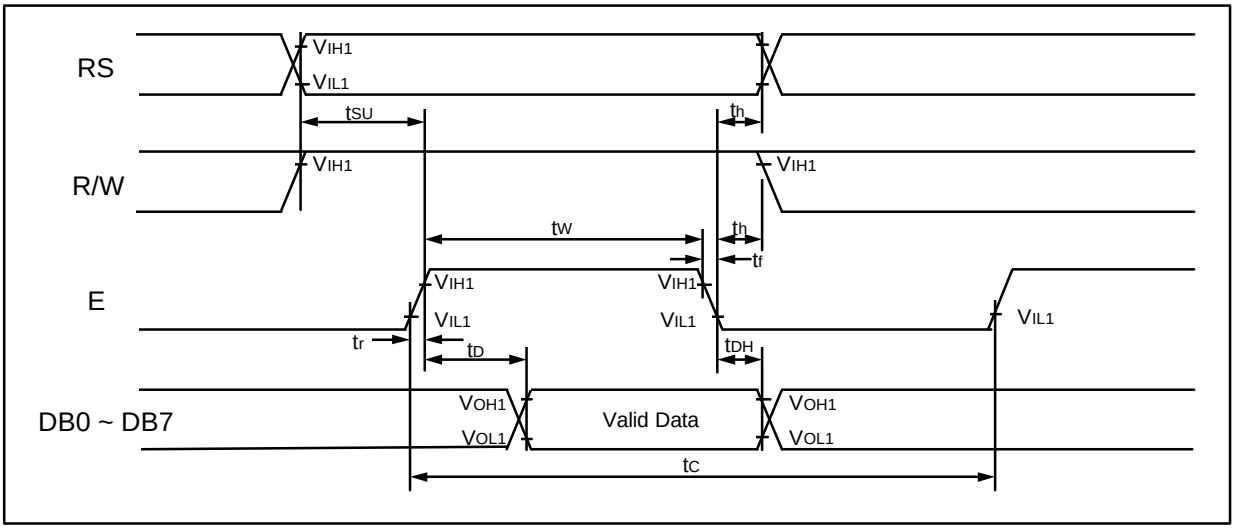



**Fig-4. Read Mode Timing Diagram**

**Table 5. CGROM Character Code Table**

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | |
| 2 | | | | | | | | | | | | | | | | |
| 3 | | | | | | | | | | | | | | | | |
| 4 | | | | | | | | | | | | | | | | |
| 5 | | | | | | | | | | | | | | | | |
| 6 | | | | | | | | | | | | | | | | |
| 7 | | | | | | | | | | | | | | | | |
| 8 | | | | | | | | | | | | | | | | |
| 9 | | | | | | | | | | | | | | | | |
| A | | | | | | | | | | | | | | | | |
| B | | | | | | | | | | | | | | | | |
| C | | | | | | | | | | | | | | | | |
| D | | | | | | | | | | | | | | | | |
| E | | | | | | | | | | | | | | | | |
| F | | | | | | | | | | | | | | | | |